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Fabrication of Photovoltaic Laser Energy Converter by MBE

Hamilton Lu, Scott Wang,
and W. S. Chan
Electro-Optek Corporation
Torrance, California

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PROJECT SUMMARY

A laser-energy converter, fabricated by molecular beam epitaxy (MBE), has been developed. This converter is a stack of vertical p-n junctions connected in series by low-resistivity, lattice matched $CoSi_2$ layers to achieve a high conversion efficiency.

Special high-temperature electron-beam (e-beam) sources have been developed especially for the MBE growth of the junctions and $CoSi_2$ layers. Making use of the small (< 1.2%) lattice mismatch between $CoSi_2$ and Si layers, high-quality and pinhole-free epilayers have been achieved, providing a capability of fabricating all the junctions and connecting layers as a single growth process with one pumpdown. The n- and p-type doping of Si layers have been made by conventional effusion sources. During development, single p-n junction, $CoSi_2$ and sandwiched layers have been fabricated and tested separately and together. Boron was used for the p-type while Sb for the n-type dopant. Well-defined multiple p-n junctions connected by $CoSi_2$ layers was accomplished by employing a low growth temperature ($\leq$ 700 °C) and a low growth rate (< 0.5 μm/hr). Producing negligible interdiffusion, the low growth temperature and rate also produced negligible pinholes in the $CoSi_2$ layers. Under these conditions, the typical growth run took over eight hours to fabricate a stack of two to four p-n junctions. For the first time a stack of three p-n junctions connected by two 10^{-5} Ω-cm $CoSi_2$ layers has been achieved meeting the high conversion efficiency requirement. Except for the low growth rate, the MBE growth of a high-quality converter has been demonstrated. This process can now be optimized for high growth rate to form a practical converter with ten p-n junctions in the stack.

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1.0 INTRODUCTION

1.1 Power dispensing in space

Large quantities of electric power can be transmitted through space to spacebased users by first collecting energy from the sun, converting it to a laser beam, and dispensing the laser energy to the spacebased users.[1] This concept, illustrated in Fig.1.1.1, involves pumping a high-energy laser by the sun in space and beaming the resultant laser energy onto a compact but efficient laser-energy converter, attached to the user, converting the received laser energy to electric power. To be practical to the spacebased users, the converter must be light-weight, efficient and low volume.

Dispensing power from a centralized space power station to distributed laser-energy converters attached to spacecrafts will simplify future spacecraft structures, enhance design flexibility, reduce drag and provide a constant energy source, even when the user is in the earth's shadow.

1.2 Laser-energy converter concept

Recent studies of energy converters made by Walker et al[2] have shown that a conversion efficiency >50% is achievable by multiple vertical p-n junctions, optimized to convert neodymium laser power with power density as high as $1x10^3$ watts/cm^2. Distinguished from the conventional planar one, this converter, illustrated in Fig. 1.2.1, is structured with its p-n junctions connected in series rather than in parallel by low-resistance paths. When in use, the multiple vertical junctions of the converter illuminated on a localized area by the laser as shown in Fig. 1.2.2, will generate an photocurrent in series with the p-n junctions, thus the power generated will be $I_p x N x V_{bi}$ watt, where I_p is the photocurrent, N the number of p-n junctions and V_{bi} is the effective built-in voltage of each p-n junction. Clearly, the conversion efficiency will be limited if I_p is limited by the series resistances connecting the junctions.

To realize high conversion efficiency, Walker[2] has predicted that the effective series resistance of the connecting paths must be less than 10^{-2} ohms. In this program, we have developed a special molecular beam epitaxy (MBE) method replacing the conventional fabrication of the multiple p-n junctions and series connecting paths to achieve specifically the low series resistance, compactness and the batch processing required.

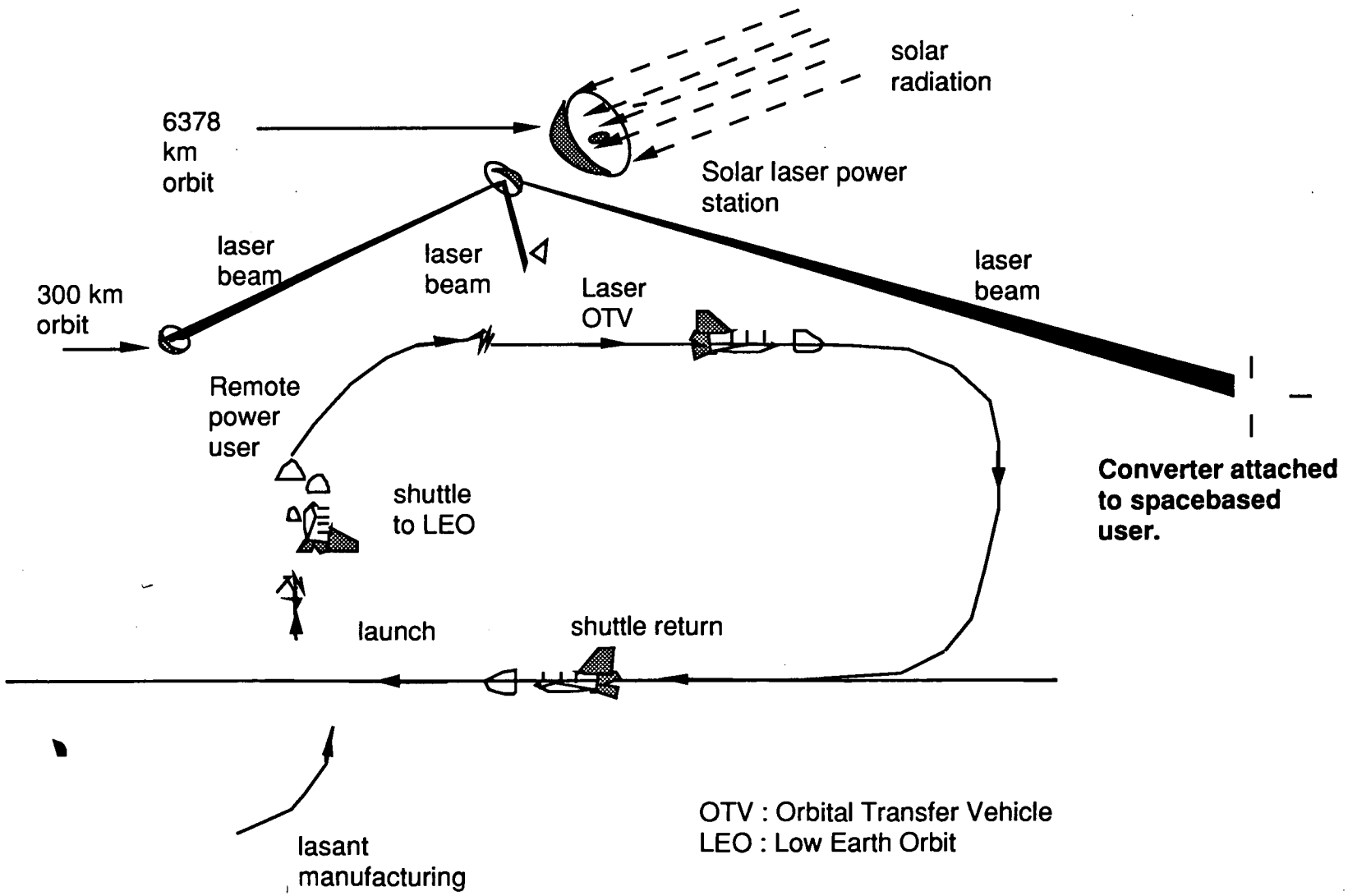


Fig. 1.1.1. Operational concept of a solar-pumped laser power station in space.

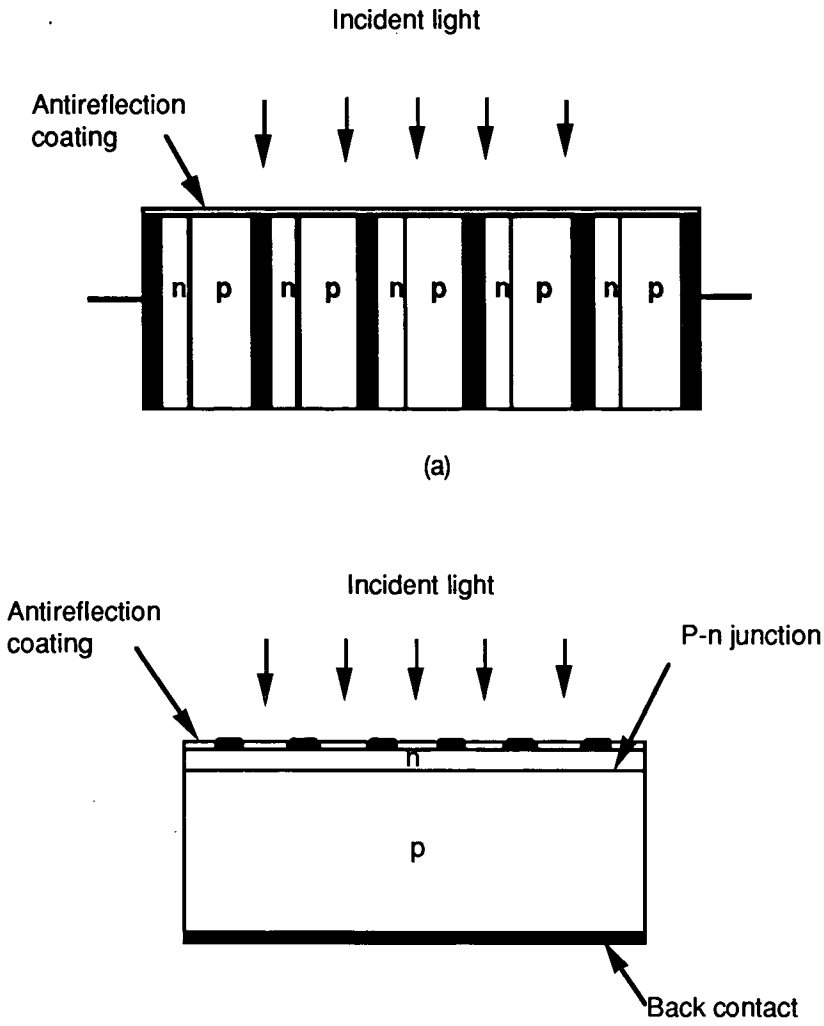


Fig. 1.2.1 Configurations of laser-energy converter. (a) Vertical multiple p-n junction type (b) Conventional planar junction type

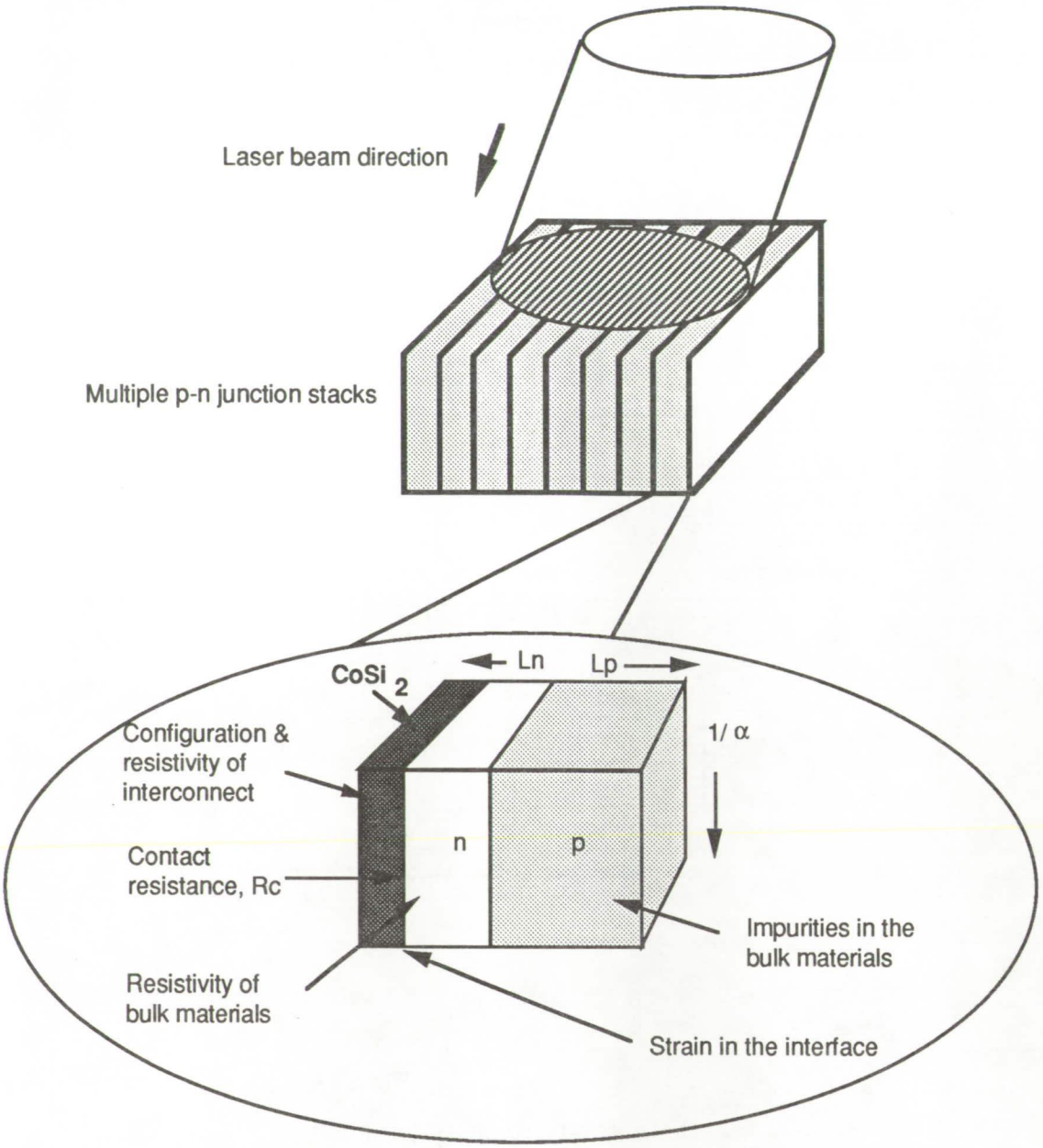


Fig. 1.2.2. Multiple p-n junctions forming the photovoltaic converter.

1.3 Program objective

The objective of this program is to demonstrate the feasibility of using molecular beam epitaxy (MBE) to fabricate multiple vertical silicon (Si) p-n junctions connected in series by low-resistivity epitaxial layers of cobalt silicide ($CoSi_2$) to form a compact and lightweight converter.

To guide the development, we have established a set a p-n junction and laser parameters, shown in Table 1.3.1, as a starting point. These are the typical parameters used by Walker [2] in optimizing the multiple vertical junctions for high conversion efficiency.

Table 1.3.1 Parameters for optimized converter

Parameter	**Value**
Series resistance	$1x10^{-2}\ \Omega$
Heat pipe temperature	20 °C
Heat-transfer coefficient	40 cal s^{-1} cm^{-2} $°C^{-1}$
Recombination velocity on n surface	$\leq$100 cm s^{-1}
Recombination velocity on p surface	$\leq$100 cm s^{-1}
Input power	$1x10^{3}$ W cm^{-2}
Laser wavelength	1.06 μm
Converter thickness	$1.5x10^{-1}$ cm
Converter width	20 μm
Converter length	1 cm
Width of the p region	4 μm
Accepter carrier concentration	$1x10^{17}$ carriers cm^{-3}
Donor carrier concentration	$1x10^{17}$ carriers cm^{-3}
Reflection coefficient	0.05
Shunt resistance	$1x10^{6}\ \Omega$

1.4 Choice of molecular beam epitaxy

By choosing MBE we have made use of several established Si MBE techniques:

1. Device-quality Si epitaxy has been established on 4 - 6 inch wafers.

2. In-situ doping to achieve n- and p-type Si epitaxial layers has been demonstrated.

3. Sequential epitaxy of p- and n- epitaxial layers forming a high-quality p-n junction has been made.

4. Single-crystal $CoSi_2$ epitaxial layer has been established.

1.5 Special processes developed

Building on the established MBE techniques, we have developed the following special processes to demonstrate the converter fabrication feasibility:

1. A low-temperature growth process with controlled epitaxy for well-defined p- and n-layers of high crystallinity and low interdiffusion has been developed to achieve thin (typically 4 microns) p-n junctions required for high efficiency.

2. High-rate dopant sources of B and Sb have been developed for in-situ doping to achieve a concentration > 10^{17} /cm^3 for high efficiency.

3. A low-temperature growth process with low contamination to prevent interdiffusion. has been developed for multiple p-n junctions growth under one pumpdown.

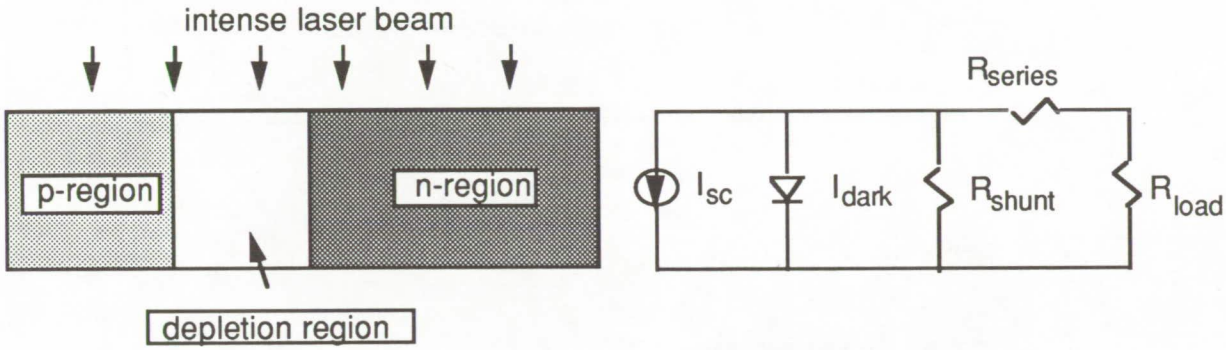
4. Epitaxy of pinhole-free $CoSi_2$ layer with a low series resistance < 10^{-3} ohm has been developed with special e-beam sources.

5. Sequential growth of $CoSi_2$ and p-n junctions with low lattice mismatch, low growth temperature, low interdiffusion and high growth rate made under one pumpdown has been developed for stack formation.

2.0 PROBLEMS TO BE SOLVED

2.1 Series resistance

The vertical p-n junction model described by Walker et al[1] is illustrated in Fig. 2.1.1(a), while 2.1.1(b) is the junction's small signal equivalent circuit. The model revealed that a conversion efficiency of >50% is achievable only if the series resistance (R_{series}) is reduced to $<1x10^{-2}$ ohm and the junctions are illuminated by lasers with a power density $>10^3$ W/cm^2, as shown in Fig. 2.1.2. Degenerately-doped Si layers cannot provide the low series resistance connecting the multiple p-n junctions because it is impractical to dope Si to degeneracy by MBE and to grow a high-quality p-n junction on top of a degenerately-doped layer. The best low resistance is a metallic-like layer. But it must be single crystal so that a single-crystal p-n junction can be grown on it to form the multiple-junction stack.



(a) Vertical junction geometry (b) Small signal equivalent circuit

Fig. 2 1.1 Model of the vertical junction.

The MBE grown silicides such as Co, Ni, Pd and Pt silicides, described in Table 2.1.1, are possible candidates for the metallic-like layer. $CoSi_2$, the best choice[2] based on crystallinity, MBE fabricability and low resistivity, have been specially developed for this effort. Investigated for other applications such as metal-base transistors and infrared detectors, it has a significant established data base to help us in this program.

Typically, $CoSi_2$ layer forms a Schottky barrier with Si, producing a contact resistivity determined by:

$$R_c=\frac{\kappa}{qA^*T}\exp\left(\frac{q\phi_{Bn}}{\kappa T}\right) \qquad (2.1)$$

where R_c is the contact resistivity, A* Richardson's constant, and ϕ_{Bn} the Schottky barrier height, q charge, k Boltzmann's constant, and T temperature. Since the barrier is typically less than 0.3 eV, the contact resistivity < 10^{-3} ohm-cm is easily achievable.

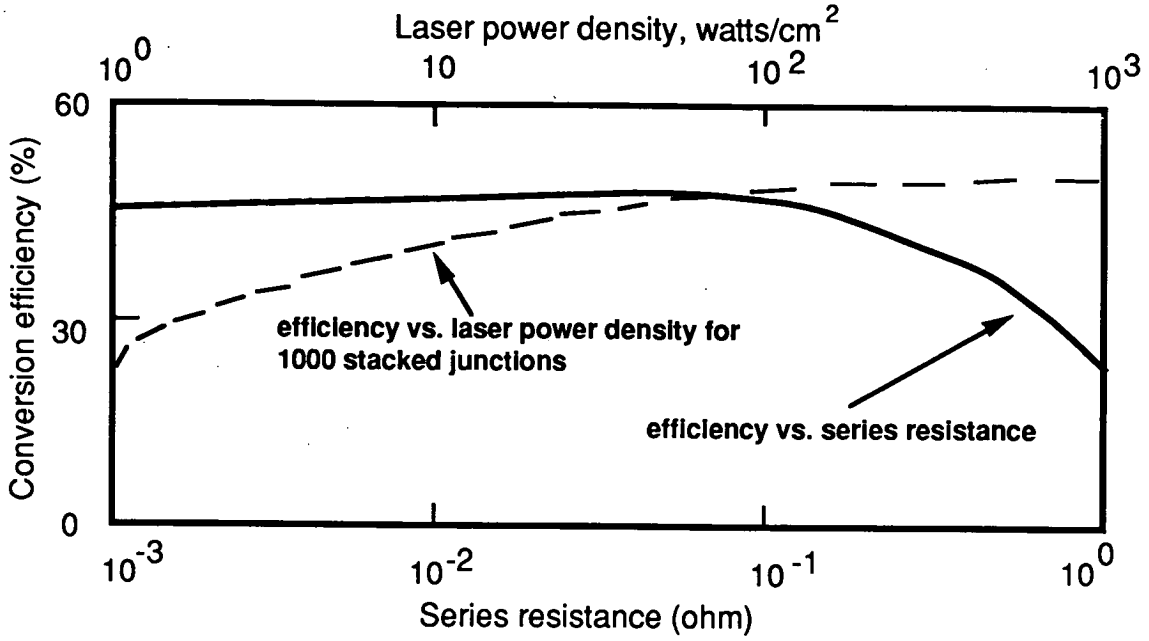


Fig. 2.1.2 Converter efficiency vs. series resistance and laser power density.

Table 2.1.1. Basic properties of some epitaxial silicides.

Silicides	$CoSi_2$	$NiSi_2$	Pd_2Si	PtSi
Structure	Cubic	Cubic	Hexagonal	Orthorhombic
Lattice constant (Å)	5.365	5.406	6.49	5.595
Mismatch with Si	1.2%	0.4%	2.4%	9.5%
Resistivity (10^{-6} ohm-cm)	2.6	20	25	35
MBE fabricability	Good	Good	Unknown	Unknown

2.2 Pinholes in $CoSi_2$ layer

MBE growth of $CoSi_2$ on Si though established,[3] epitaxial layers invariably contained a high density of pinholes, induced by lattice mismatch, particulates depositing on substrate surface during epitaxy, uneven local heating of the substrate and uneven growth rates.

High-temperature e-beam sources and low growth temperature processes have been developed for this project especially to reduce the occurrence of pinholes and to keep the interdiffusion down to a low level.

2.3 Thin multiple p-n layers

Multiple layers, each about a few microns thick, are required to form the vertical-junction converter structure. Given the low MBE growth rates, a long growth period will be required. As such, high growth stability is required for multiple-junction epitaxy.

Special e-beam and effusion sources have been developed here to achieve a high growth stability over a long period.

The optimum thickness of each p-n junction of the multiple-junction stack for high conversion efficiency is about 4 micron, as shown in Fig. 2.3.1. Thinner p-n junctions will cause an necessary loss of photon absorption reducing the conversion efficiency, while thicker junctions will create high series resistance and a longer time for multiple-junction growth.

MBE growth of 4-micron p-n junctions has been developed for this program. Such thin junctions required a low-temperature growth process to prevent interdiffusion.

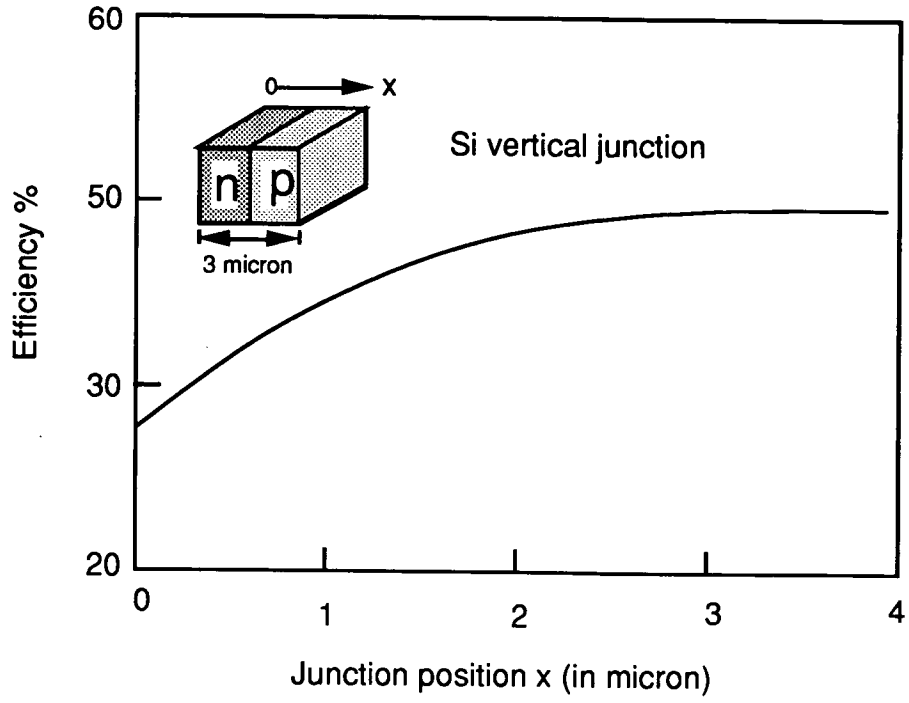


Fig. 2.3.1. Efficiency of a vertical Si p-n junction vs. junction thickness (or position).

2.4 Lattice mismatch

Due to the lattice mismatch with Si, the Si/$CoSi_2$/Si heterostructures required for the vertical junctions are difficult to fabricate. Although this mismatch may not increase the layer resistance materially, the interfacial defects may increase the interfacial recombination velocity, which will in turn decrease the conversion efficiency of the vertical junction.

We have developed a low-temperature growth in combination with an annealing process conducted in tandem to reduce the interfacial defects and series resistance at the same time.

2.5 Doping profile control

An abrupt doping profile is required for the formation of a well-behaved p-n junction. Growing a single p-n junction by MBE is relatively straightforward, but when a stack of multiple junctions having the same profile is fabricated interdiffusion will take place, unless a special epitaxial process is established to mitigate that.

We have developed a low-temperature growth process to grow p-n junctions in tandem with controlled abrupt doping profiles to reduce interdiffusion of the dopant species during growth.

2.6 Prolonged multilayer growth

The MBE growth a multilayer stack of p-n junctions connected by $CoSi_2$ layers will required many hours of prolonged growth using the typical MBE growth rate of <1 micron/hour. Prolonged growth causes: (1) contamination of the growth chamber due to heating of chamber walls; (2) non-uniformity of the doping profile due to uneven growth temperature over the substrate and in the MBE sources; and (3) loss of dopant and MBE material sources leading to loss of growth continuity. Establishing MBE processes and sources for a high rate of growth will eliminate most of these problems. However, a high rate of growth is not conducive to well-ordered epitaxy which usually occurred at an optimally slow rate, and a high effusion rate from a high-temperature MBE source will cause uneven heating and over heating of chamber fixtures leading to cross contamination.

A low-temperature growth technique along in conjunction with an annealing process have been developed here to achieve high quality epitaxy under prolonged growth. To reduce cross contamination caused by over heating of the chamber walls, we have designed the MBE chamber with cooled walls and low-surface fixturing, as shown in Fig. 2.6.1.

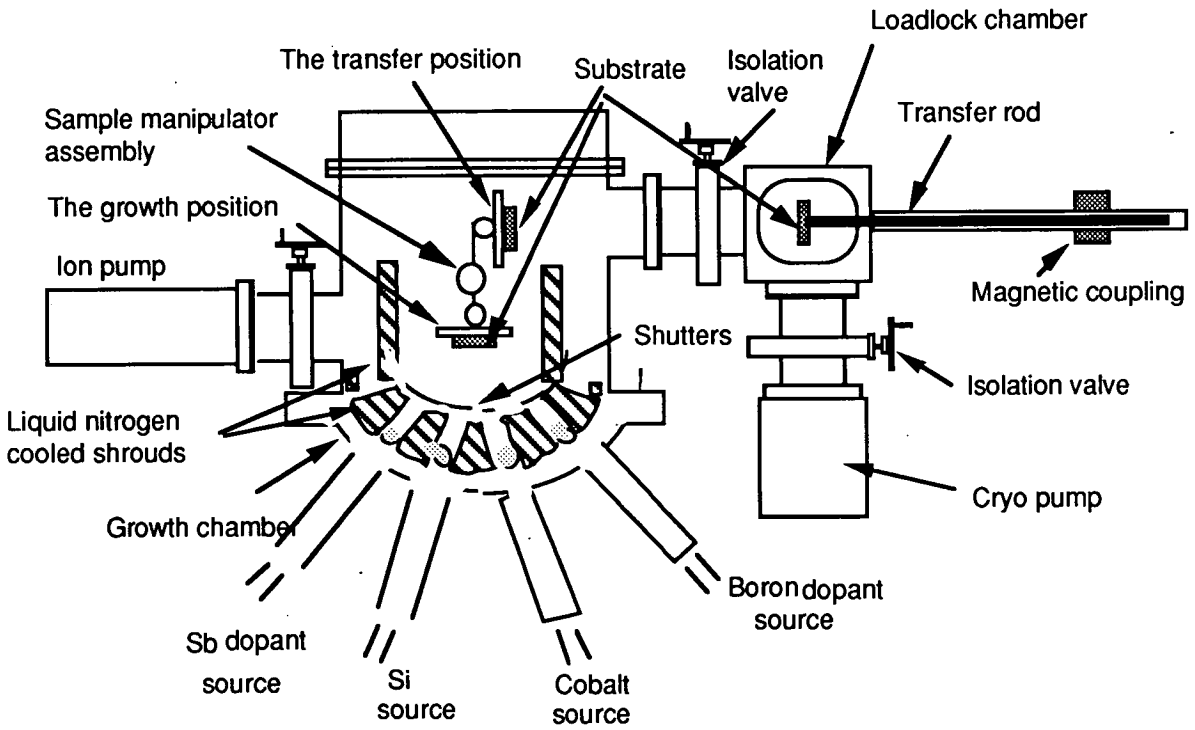


Fig. 2.6.1 MBE chamber designed with cooled walls and low-surface fixturing.

3.0 SPECIAL MBE TECHNIQUES

To meet the objective of this program, we have designed special MBE sources and fixtures for our existing MBE system to solve the problem discussed in the last section. Fig. 2.6.1 shows a layout of the MBE system used for this program.

3.1 Special MBE fixtures

The major modifications made on our existing system were:

1. Incorporation of a 3-inch sample manipulator in the growth chamber,
2. Incorporation of a liquid nitrogen cold shroud inside chamber,
3. Incorporation of e-beam sources for Co and Si.

3.2 3-inch sample manipulator

To achieve uniform and prolonged growth, a rotary sample holder was designed to hold a 3" Si wafer, as shown Fig. 3.1.1, showing the holder structures and the various operating configurations. During wafer transfer, the holder was held in upright position shown in Fig. 3.1.1(a). During growth, the holder was rotated to the down position with the substrate situated about 15 cm from the effusion sources, as shown in Fig. 3.1.1(b). After growth the holder was again rotated to the upright position, allowing the wafer to be transferred out of the chamber. In the upright position, the holder was held fast and steady by a hook making the wafer transfer easier.

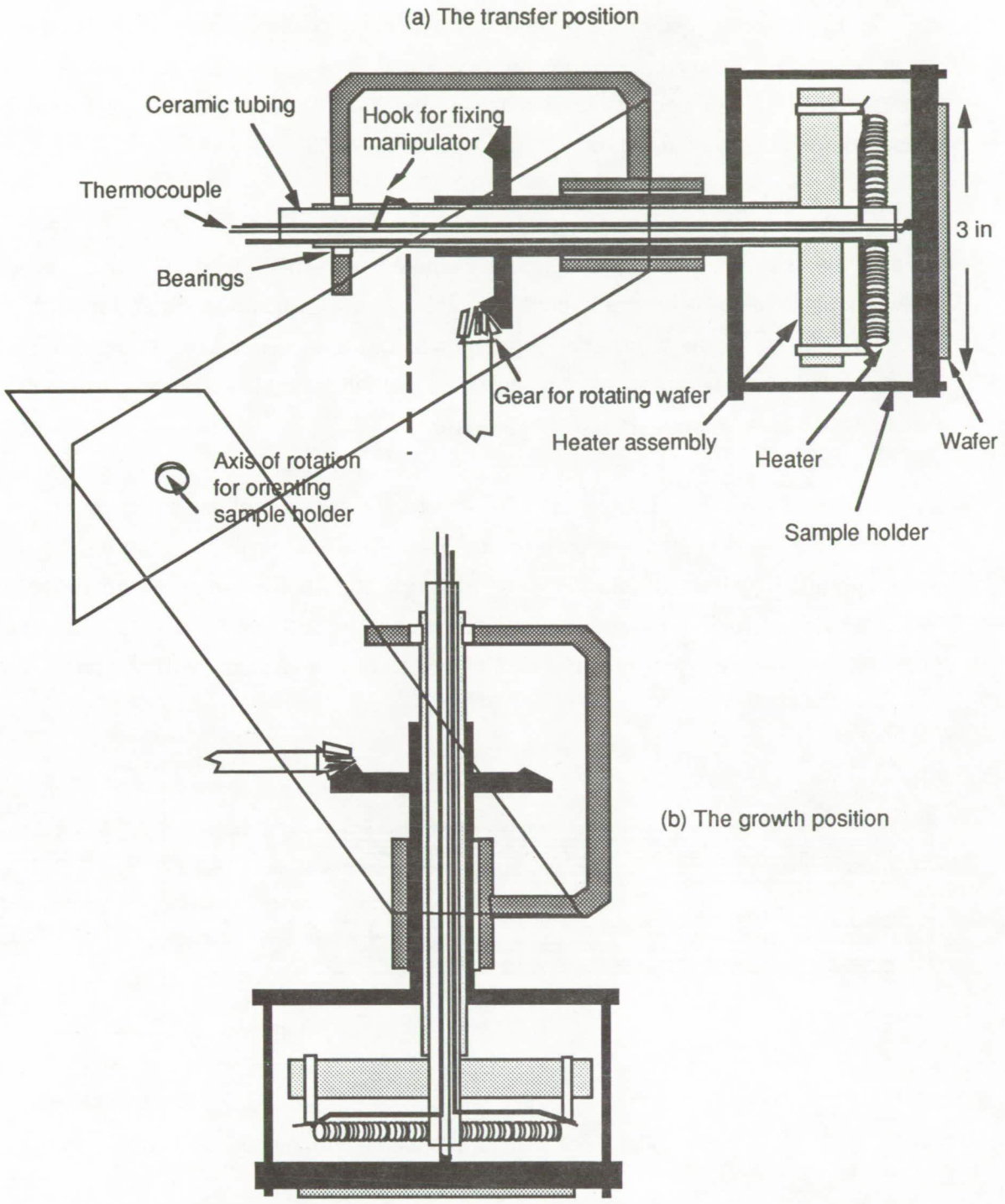


Fig. 3.1.1(a) and (b) Two positions of wafer holder: wafer transfer position and film growth position

3.3 Liquid nitrogen cold shroud

Liquid nitrogen cold shrouds were arranged around the growth position of the wafer holder. During prolonged growth, the shrouds were cooled to 77K acting as cold traps of evaporated

specifies to prevent secondary evaporation, thus reducing chamber cross contamination.. These shrouds were necessary because during prolonged growth periods the temperature of the chamber walls if not cooled could reach as high as 600°C, high enough for secondary evaporation, undesirable for epitaxy.

3.4 E-beam sources for Co and Si

E-beam sources were specially designed to evaporate high-melting point Co and Si, for which conventional effusion cells would not be suitable. This was the most difficult modification of the MBE system, for the chamber configuration had to be modified to accommodate the larger components and the sources had to be designed and fabricated from scratch, which meant all functions had to be thoroughly tested before use.

Conventional MBE systems use effusion cells to generate molecular beams. The typical structure of a Knudsen cell is shown in Fig. 3.4.1. When a pyrolytic boron nitride (PBN) is used with this Knudsen cell, the cell's useful temperature range can extend to about 1100°C. When a carbon crucible is used the temperature can be as high as 1400°C. However, this temperature is not sufficient to evaporate Co or Si, even in a vacuum of 10^{-11} Torr.

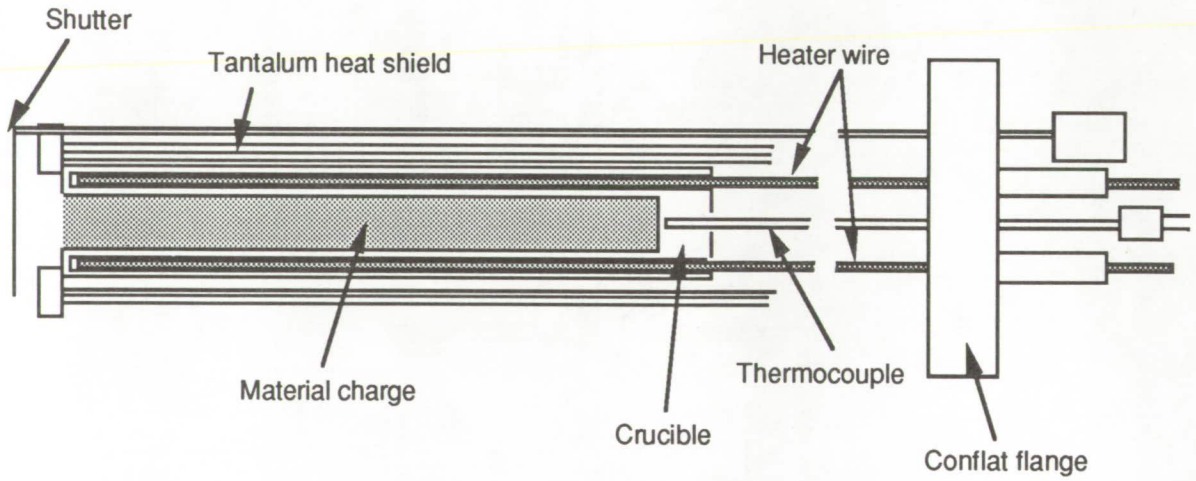


Fig. 3.4.1. The structure of a conventional effusion cell.

E-beam evaporator sources had to be used for Co and Si for high temperatures of about 2000°C and 1400°C for Co and Si, respectively. In addition to the high temperature capability, the e-beam sources when operated properly would produce less outgassing. A comparison of the background gas constituents evolved from an e-beam source and from an effusion cell for Si is given in Fig. 3.4.2. Clearly, the effusion cell produced much higher outgassing contamination than the e-beam source.

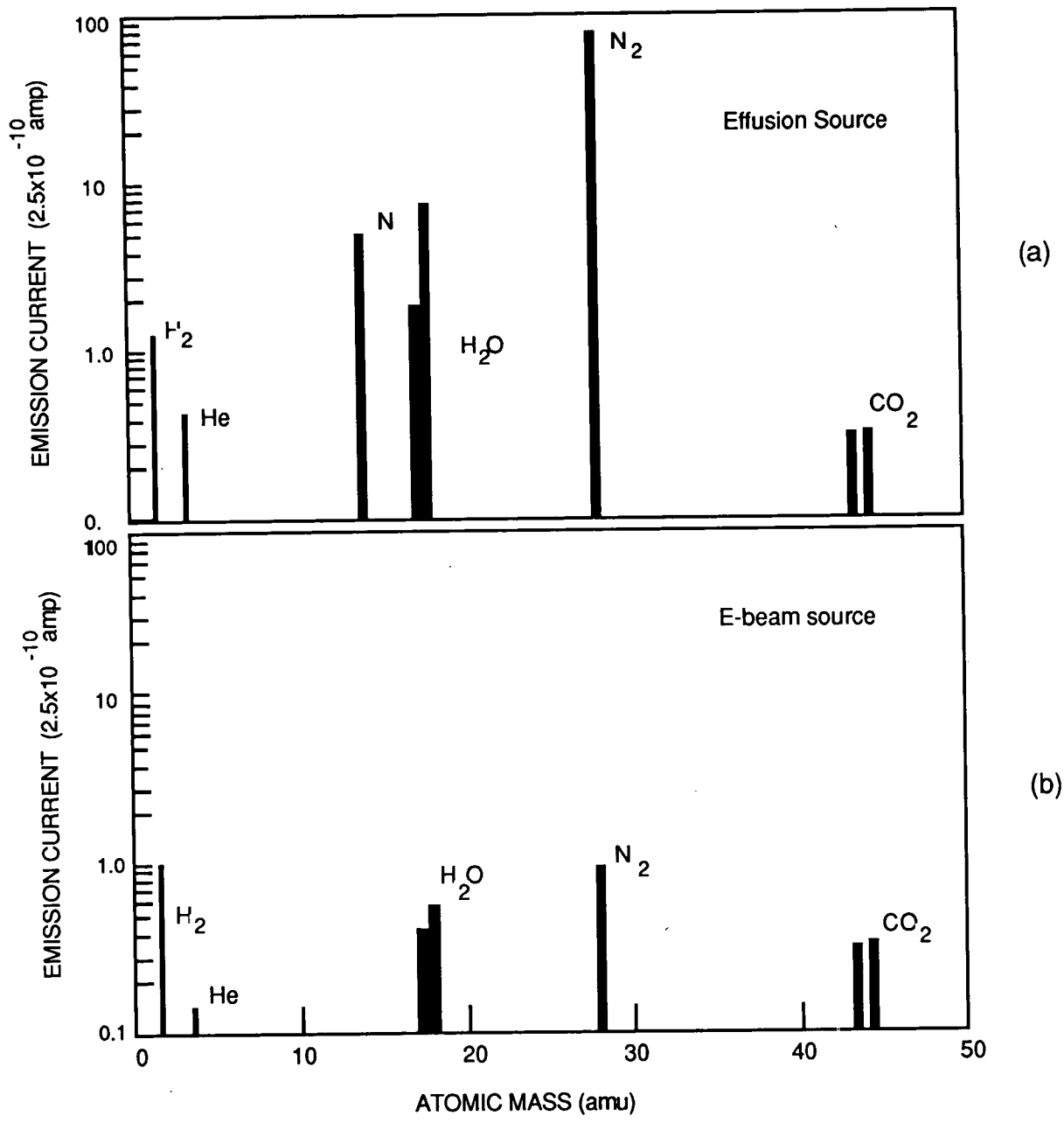


Fig. 3.4.2. Outgassing comparison between the e-beam and effusion sources.

The operational principle of e-beam source is straightforward. Electrons emitted from a heated filament at about -4 kV potential relative to the source material heat and melt the source material, as shown in. Fig. 3.4.3 and Fig. 3.4.4. The latter shows how the e-beam sources are configured within the growth chamber. The source material is situated on the top of a feedthrough which is used to drive the source material into the melting zone of the e-beam.. As the source material is being used, the feedthrough is push further into the chamber so the

material source will always be located at the melting zone. The detailed structure of the e-beam emitter is shown in Fig. 3.4.5.

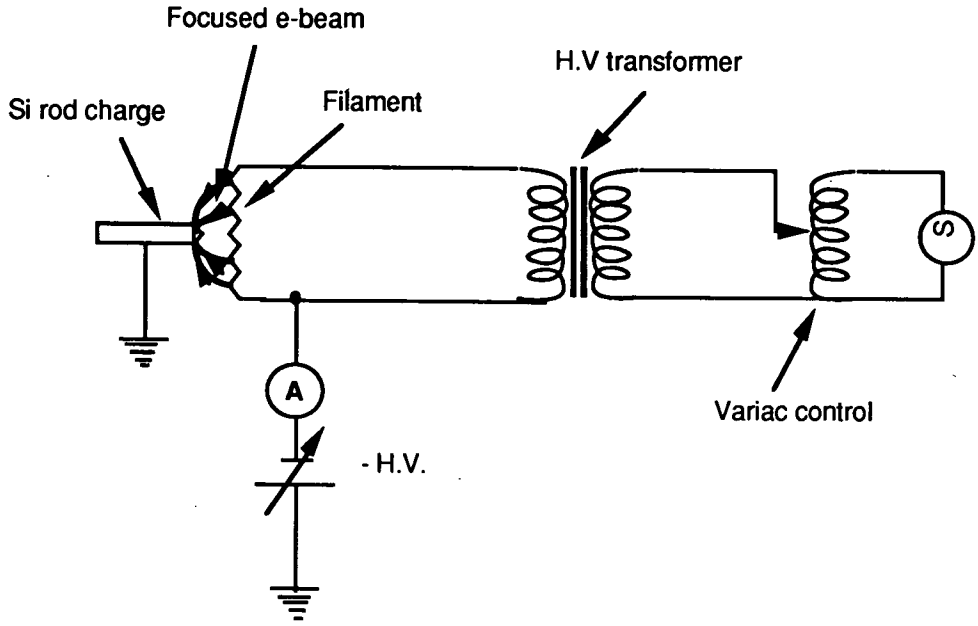


Fig. 3.4.3 Equivalent circuit of e-beam evaporator source.

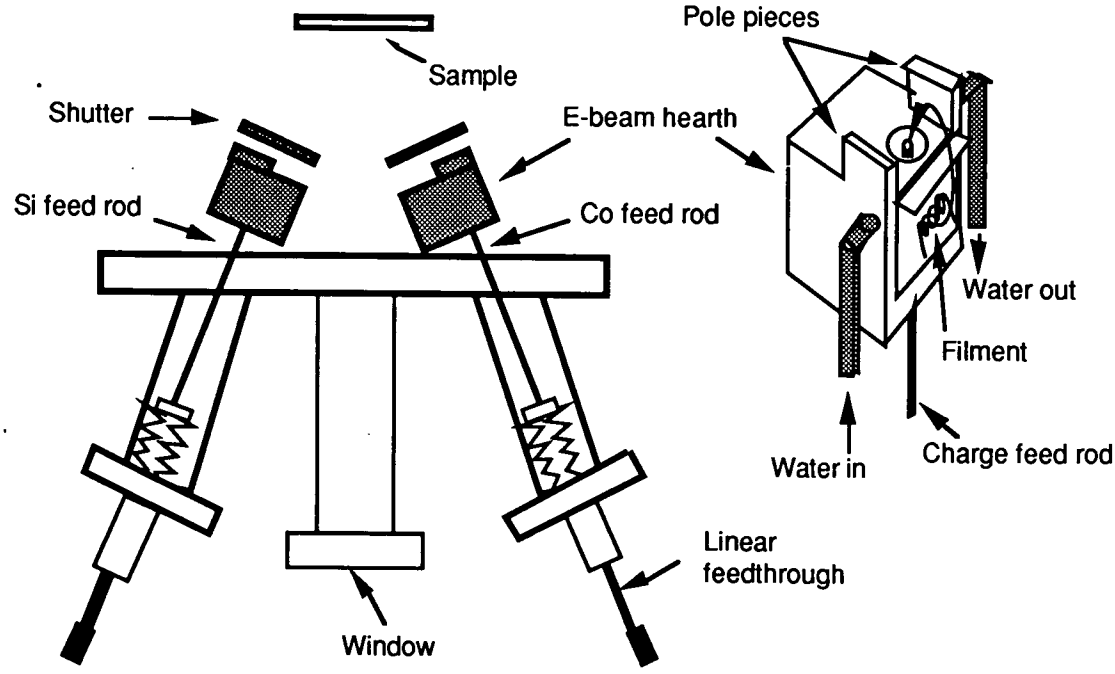


Fig. 3.4.4 Configuration of e-beam evaporator source.

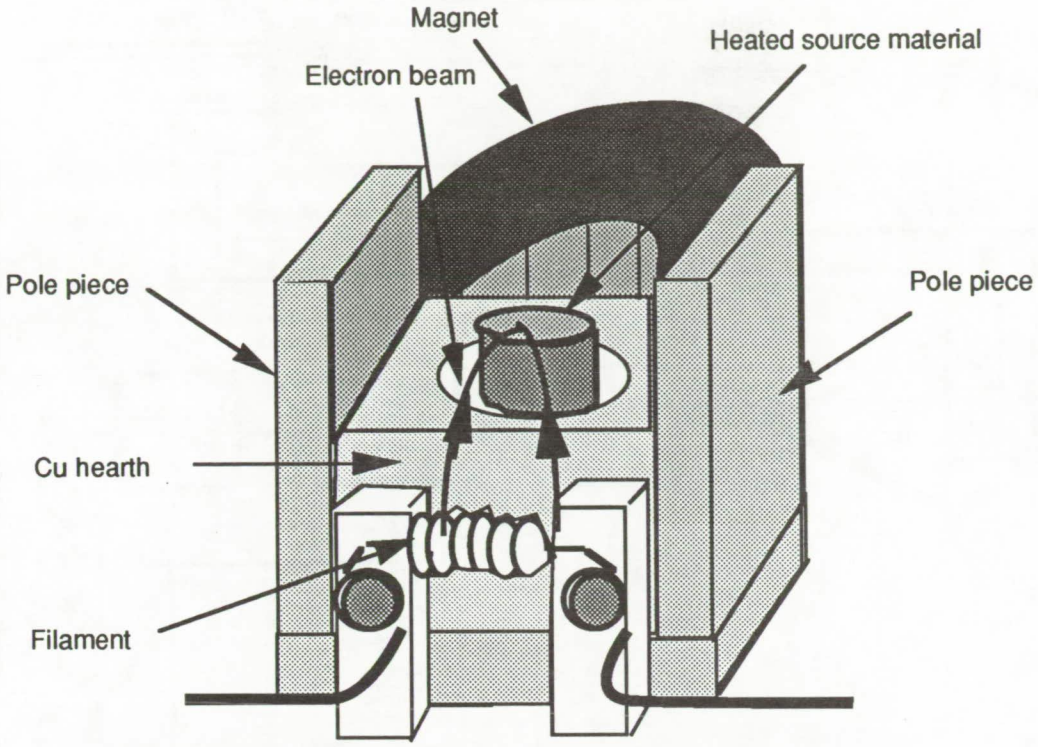


Fig. 3.4.5. Hearth configuration of e-beam evaporator source.

The focusing of electrons is accomplished by adjusting metal shields, bias potential of the filament, and emission current of the evaporator. The growth rate using the e-beam source was about 0.1 micron per hour. A stable power supply shown in Fig. 3.4.6 was necessary for prolonged growth.

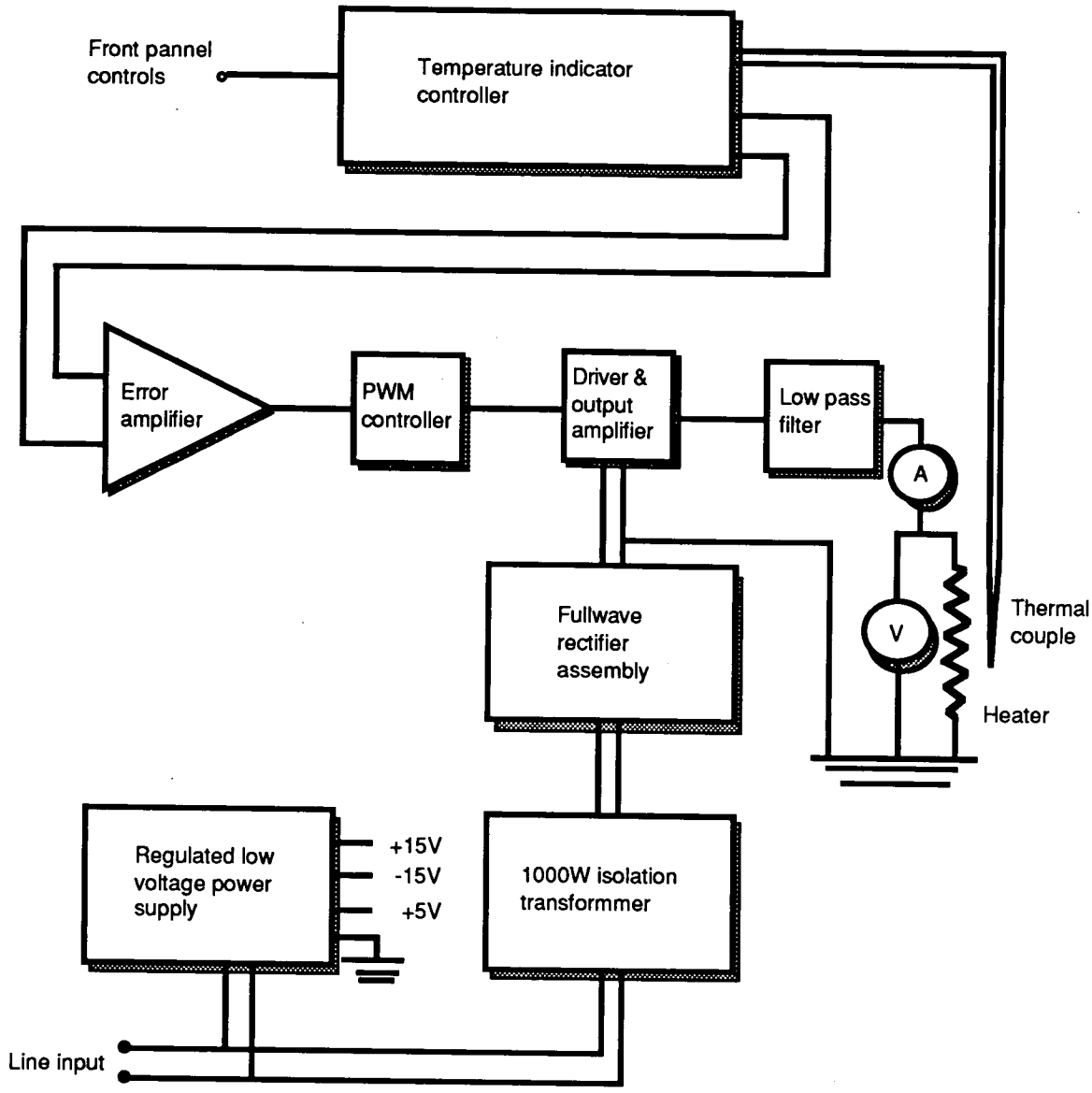


Fig. 3.4.6 Diagram of stabilized DC power supply for e-beam source.

4.0 MULTILAYER GROWTH TECHNIQUES

4.1 Reduction of series resistance using $CoSi_2$

Due to a small lattice mismatch with Si, $CoSi_2$ fabricated by co-evaporation under MBE conditions has produced low resistivity and a low Schottky barrier height. It also possesses good temperature stability to survive the MBE fabrication process.

The resistivity of grown $CoSi_2$ varied from 8 to 35 $\mu\Omega$-cm at room temperature depending on the preparing process of the films. Temperature stability of grown materials was important since the process might go through extensive temperature cycling. After a 5-hour heating at 800°C, the material structure of $CoSi_2$ remained basically unchanged and showed little or no interdiffusion.

4.2 In-situ doping profile by MBE

In-situ doping Si with B and Sb impurities to form p-n junctions was the major part in making the multiple vertical p-n junction stacked converter. In-situ doping was accomplished by co-depositing boron (p-type doping) or antimony (n-type doping) from conventional effusion cells during the epitaxy of Si. The Si flux was generated by e-beam evaporation of high purity (99.999%) Si rod. The desired doping concentration was achieved by properly adjusting the arriving molecular flux ratio of dopant to Si. The dopant fluxes were controlled by the cell temperature, whereas the Si and Co fluxes were determined by the biasing voltage applied to the filaments and the emission currents of the evaporator sources.

The doping concentration of the dopant in Si was determined by Hall or SIMS measurements. The set up for Hall measurement is shown in Fig. 4.2.1. Carrier concentration, mobility, and resistivity were obtained by following standard Hall measurement, correction, and calculation procedures.

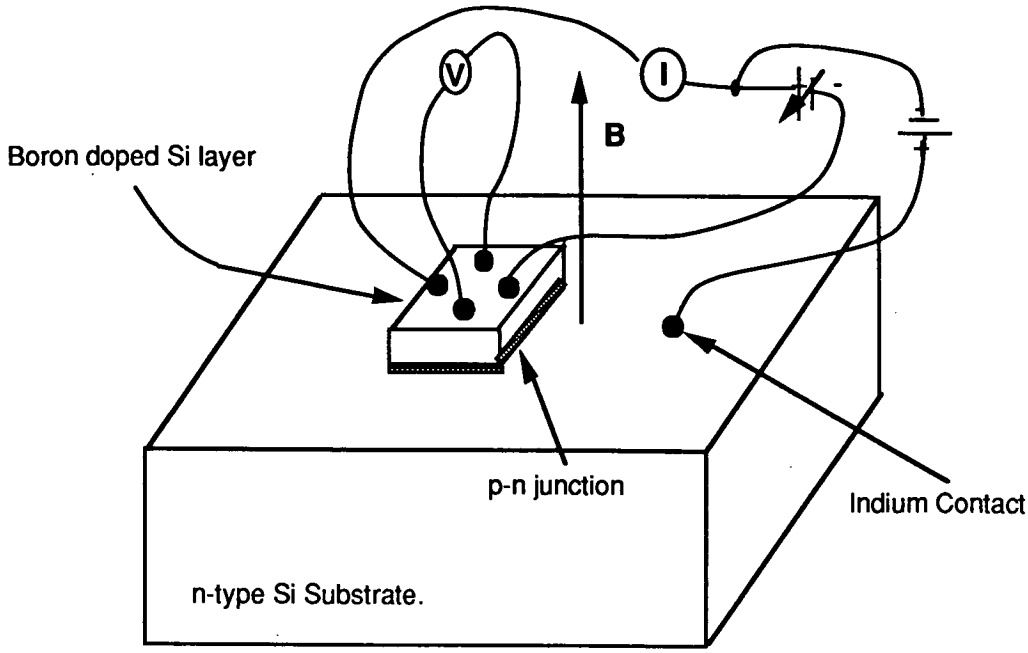


Fig. 4.2.1 Hall measurement setup

The SIMS measurement could determine the impurity levels with higher accuracy than the Hall measurement, but the concentration obtained was the actual number of impurities rather than the electrically active impurities. We will see in the next section, impurity concentration profiles resulted from SIMS analysis were used to verify the structures of fabricated devices.

4.3 Low-temperature process

We have investigated two major temperature effects in the fabrication process: the peak temperature of the MBE growth of one layer affecting the epitaxial quality of the subsequent layer, and the repeated and prolonged heating of the substrate degrading the profile of the p-n junction being fabricated.

Extensive growth runs have established the optimum growth temperatures of 500 and 700°C for Si p-n junction and $CoSi_2$, respectively. These temperatures are considered relatively low for epitaxial growth. From the diffusion constants of boron and antimony shown in Table 4.3.1, we see that the average diffusion distance under different temperatures could be estimated.[11] Both p- and n-type doping profiles were very stable for temperature up to 800 °C. The structure of $CoSi_2$ was also stable up to 800 °C. As long as the temperature used in the growth process was kept below 800 °C, the doping profile and contacts would not be smeared by interdiffusion. In the growth process that we have optimized, both Si and $CoSi_2$ were

grown around 700 °C to assure high stability of designed doping profiles and the establishment of high crystallinity (which usually requires a high temperature).

Diffusion Coefficients for B and Sb** in Si

Element	$D_O(cm^2/sec)$	$E_V(eV)$
B	10.5	3.69
Sb	5.60	3.95

** diffusion constant $D = D_O \exp(-E_V/kT)$

Table 4.3.1 Diffusion coefficients of boron and antimony

4.4 Growth evaluation

From fabrication purposes, a double p-n junction interconnecting by a $CoSi_2$ layer can be considered as a basic unit constructing the whole multilayer converter, as illustrated in Fig. 4.4.1. If a high current output capacity is required, the basic units should be connected in parallel rather than in series. However, the fabrication of parallel basic units is not conducive to MBE techniques, and is therefore considered here. When the basic units are fabricated in a stacked form a high photovoltage will be created, but the resultant current will be smaller than the parallel combination. To fabricate the multiple junctions we have optimized three growth processes:

1 Optimize growth of one p-n junction on Si substrate,

2 Optimize growth of $CoSi_2$ on top of p-n junction, and

3 Optimize growth of multiple p-n junctions connected by $CoSi_2$ layers.

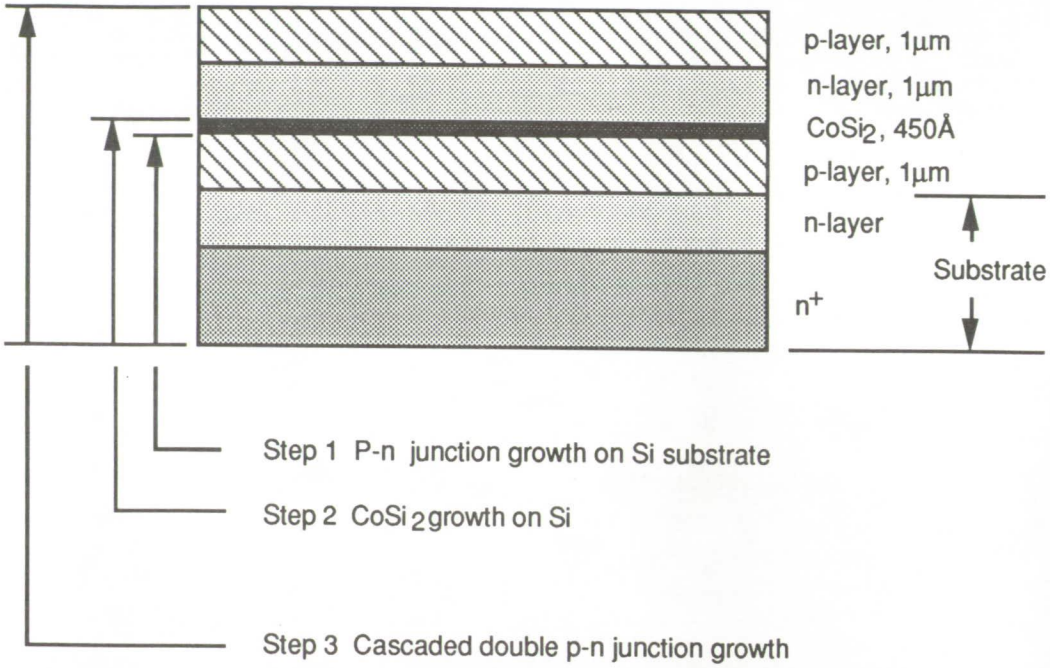


Fig. 4.4.1. Steps of multiple junction growth

After the double p-n junction was completed, its optical response was measured. The widths of p- and n-layers were set at about 1 μm only , rather than about 4 micron, because we could only achieve a growth rate of about ~0.2μm/hr due to the limitation of the e-beam rod feed. Though the source flux could be increased by increasing the e-beam power, the higher power began to cause excessive outgassing, unacceptable for prolonged growth.

4.5 P-n junction growth on Si substrate

4.5.1 Wafer cleaning

Wafers were cleaned, ex-situ and in-situ, before growth . The ex-situ cleaning procedures included degreasing, etching of wafer surface to eliminate contaminants, and passivation of wafer surface after etching. This procedure is:

(1) Rinse in overflowing deionized water for 10 minutes.

(2) Rinse twice in methanol bath for 5 minutes with agitation.

(3) Boil in chloroform bath for 15 minutes.

(4) Rinse twice in acetone bath for 5 minutes with agitation.

(5) Repeat step (2).

(6) Repeat step (1).

(7) Boil in HNO_3 bath at 130 °C for 10 minutes to etch Si surface and to form a thin oxide layer.

(8) Dip in 2.5% HF solution for 10 seconds to remove the oxide.

(9) Repeat step (1).

(10) Check the Si surface. If the surface does not dry uniformly, repeat step (7) - (9).

(11) Boil in a solution of $NH_4OH:H_2O_2:H_2O$ (1:1:3) at 90 °C for 10 minutes to form a thin oxide layer.

(12) Repeat step (8).

(13) Repeat step (1).

(14) Boil in a solution of $HCl:H_2O_2:H_2O$ (5:3:2) at 90 °C for 10 minutes to form a thin oxide layer.

(15) Repeat step (1).

(16) Check the Si surface. If the surface does not wet uniformly, repeat step (11) - (15).

(17) Blow dry with nitrogen gas.

The in-situ Si flux cleaning procedure of substrate is as follows:

(1) After ex-situ substrate preparation, the Si is immediately mounted onto the molybdenum sample holder and loaded into the load-lock chamber.

(2) Magnetically transfer sample from load-lock to MBE growth chamber.

(3) Clean substrate with a Si flux in the growth chamber at about 800 °C for 30 minutes.

(4) Change substrate temperature to 600 °C for Si layer growth.

The optimum growth conditions establi[redacted] Si epitaxy were as follows:

(1) Silicon substrate orientation: (1

(2) Base pressure: 5×10^{-10} Torr

(3) Substrate temperature: 650 °C

(4) Growth pressure: 2×10^{-8} Torr

(5) Growth rate: 0.1 μm/hour

(6) Epitaxial thickness: 1 μm per layer

(7) Surface morphology: mirror-like with no apparent surface blemishes

(8) P-type film was formed by boron doping and n-type film by antimony doping.

4.5.2 P-type Si grown by effusion sources

The growth of the B-doped Si film was made by using a conventional B effusion source. This enabled us to obtain any desired B concentration by varying the boron source temperature. The nominal B source operating temperature was 1200-1400 °C. Three growth conditions of B doped Si films were tried to calibrate the concentration profile. The substrate temperature was kept at 650 °C to avoid high temperature damage for the multiple p-n junctions. As can be seen in the next section, the n-type dopant has the tendency to re-evaporate out of the heated substrate to ruin the p-n junctions. The effusion source for Si was kept at about 1650°C which as the limit of the PBN crucible used. The higher the substrate temperature was, the worse would be the doping fluctuation. The growth rate was about 1 μm/hr at this growth temperature. Four point probe measurements were used to characterize the resultant films. B doped Si films were found to be p-type. Chemical analysis of the films made by Second Ion Mass Spectroscopy (SIMS) confirmed the boron doping concentration measured by four-point probe measurement. Fig. 4.5.2.1 shows the depth profile of the B concentration ranging from 2×10^{17} to 5×10^{19} atoms/cc for different B source temperatures with respect to different temperatures of B effusion cell.

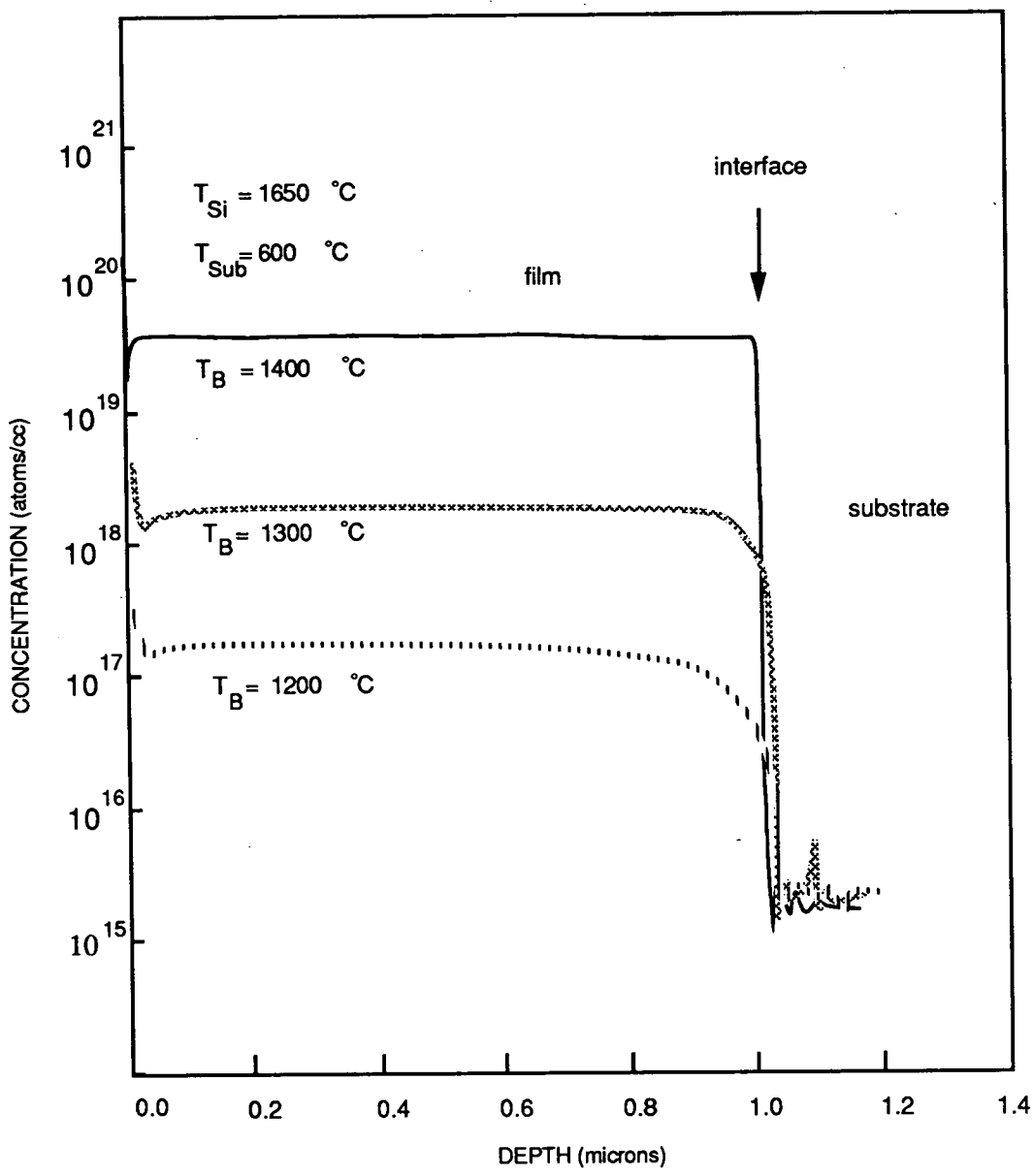


Fig. 4.5.2.1. Concentration-depth profile of a boron doped Si film measured by SIMS. T_{sub}, T_{Si} and T_B are the Si substrate temperature, Si source temperature and boron source temperature, respectively.

4.5.3 N-type Si grown by effusion sources

To calibrate Sb doping concentration, the Si substrate and Si source temperatures were maintained at 600 °C and 1650 °C, respectively throughout the growth. For the first 0.1 μm of the film, as indicated by region 1 of the depth profile of the Sb doped Si films measured by SIMS shown in Fig. 4.5.3.1, the average Sb concentration N_{Sb} was about $1x10^{17}$ atoms/cc with T_{Si} = 1650°C and T_{Sb} = 250 °C. For the next 0.2 μm of the film, as indicated by region 2, N_{Sb} was increased to $2x10^{18}$ atoms/cc because T_{Sb} was increased to 280°C. For the rest of the film, as indicated by region 3, N_{Sb} was $5x10^{18}$ atoms/cc because T_{Sb} was increased to 300 °C. The fluctuation of Sb profile was due to the re-evaporation of Sb from the heated substrate.

Unintended B doping by the PBN crucible of the Si source had also occurred. Our measurements showed some p-type characteristics. The B doping concentration originated from the PBN crucible might be compatible with the Sb concentration. It was found that the effective carrier concentration obtained from the resistivity measurement was smaller than the estimated Sb concentration obtained from SIMS. This implied that the Sb doped films were compensated, and that the p-type dopant was still the dominant species. This was the main reason for us to replace the Si effusion cell with a rod-feed e-beam source.

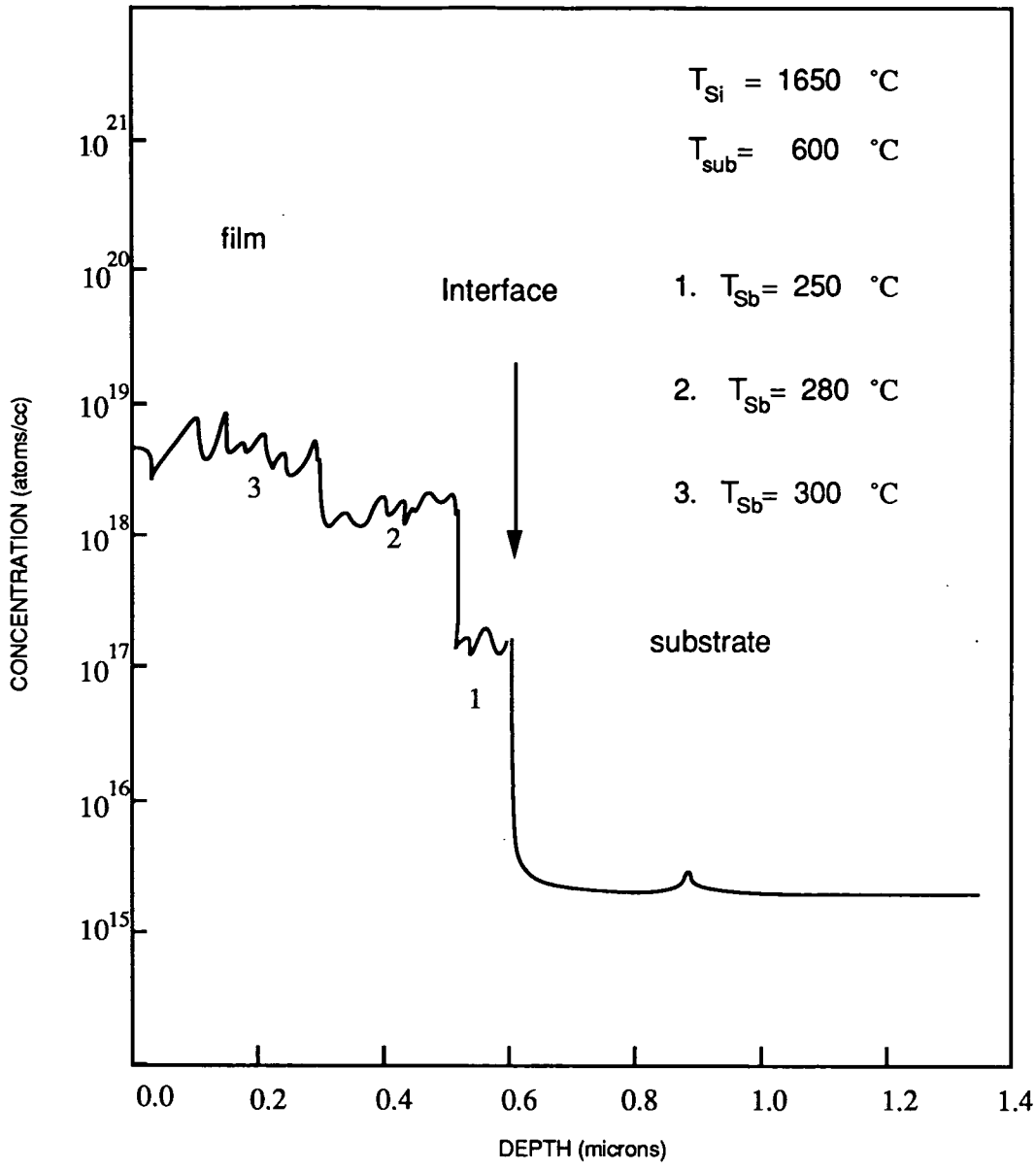


Fig. 4.5.3.1. Sb concentration depth profile of a Sb doped Si film growth using effusion sources and measured by SIMS

4.5.4 Doped Si grown by e-beam source

Two 3-KW e-beam sources were constructed for Si and Co evaporation. The typical power consumption for the Si e-beam source was about 0.3-2 KW which produced a deposition rate of 0.2-0.3 mm/hr. Since the tip of the rod-fed charge has the highest temperature and the e-beam source was water cooled, the outgassing was significantly reduced compared to the high-temperature Si effusion source. A comparison of the residual gas spectrum between the

growths using the high temperature effusion source and using the e-beam source is shown in Fig. 3.4.2 . Though the Si deposition rate using the e-beam source was 1/5 of the growth rate of Si effusion cell, the residual gas was about two order of magnitude smaller than that using the high temperature effusion source. Furthermore, the unintentional doping of boron from the PBN crucible was completely eliminated. The significant reduction of contaminants of C and N was also observed in the SIMS measurements. In Fig. 4.5.4.1, we compared depth profiles of C and N in a doped Si film grown by the high-temperature effusion source with those grown by the e-beam source. We found that overall the nitrogen concentration was down by two to three orders of magnitude and carbon concentration down by one order of magnitude when the e-beam source was used.

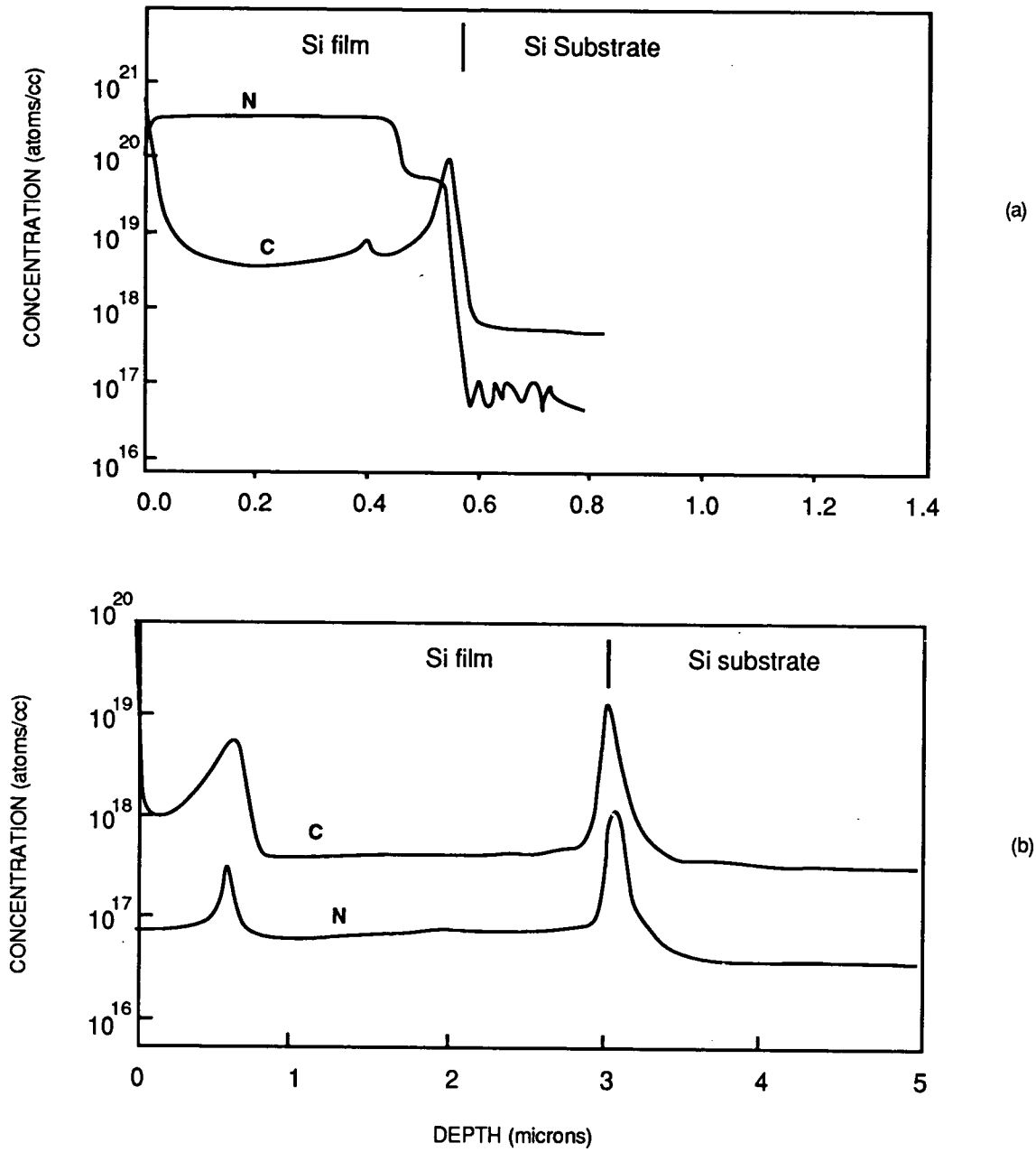


Fig. 4.5.4.1. Depth profiles of contaminants of C and N of doped Si films grown: (a) by a high temperature Si effusion source; and (b) by a Si e-beam source.

One major problem we have encountered when using the e-beam source was the heavy consumption of Si rod. We needed to change Si charge frequently, after only a few growth runs, because the 1/4" diameter rod charge used in an earlier e-beam source depleted very quickly. We have subsequently incorporated a larger-diameter, 1/2" rod charge, which increased the life time of the Si charge fourfolds.

4.5.5 In-situ doping of Si multilayers

Theoretical calculation[2] of a single Si p-n junction diode for the photovoltaic applications suggests that the optimum doping concentration and thickness for n- and p-layers were 10^{17} /cm^3 and 4 micron, respectively. Using these as guidelines in our MBE growth, an p-n structure was grown in-situ on a 3" diameter <111> p^+ Si substrate. This Si p-n structure was capped by a n^+ Si layer. The p^+ substrate and n^+ cap layer were used for ohmic contacts. A diagram of this structure is shown in Fig. 4.5.5.1 .The e-beam source was used for the Si evaporation, while the conventional effusion sources were used for the dopant B and Sb evaporation. The doping concentration could be varied by adjusting the dopant (B and Sb) to Si flux ratio, which depends on their source temperatures. The B and Sb source temperatures were operated in the range of (1000-1200) °C and (200-250) °C, respectively The Si substrate was maintained at 650 °C during the entire growth period. The growth pressure was $1x10^{-8}$ torr.

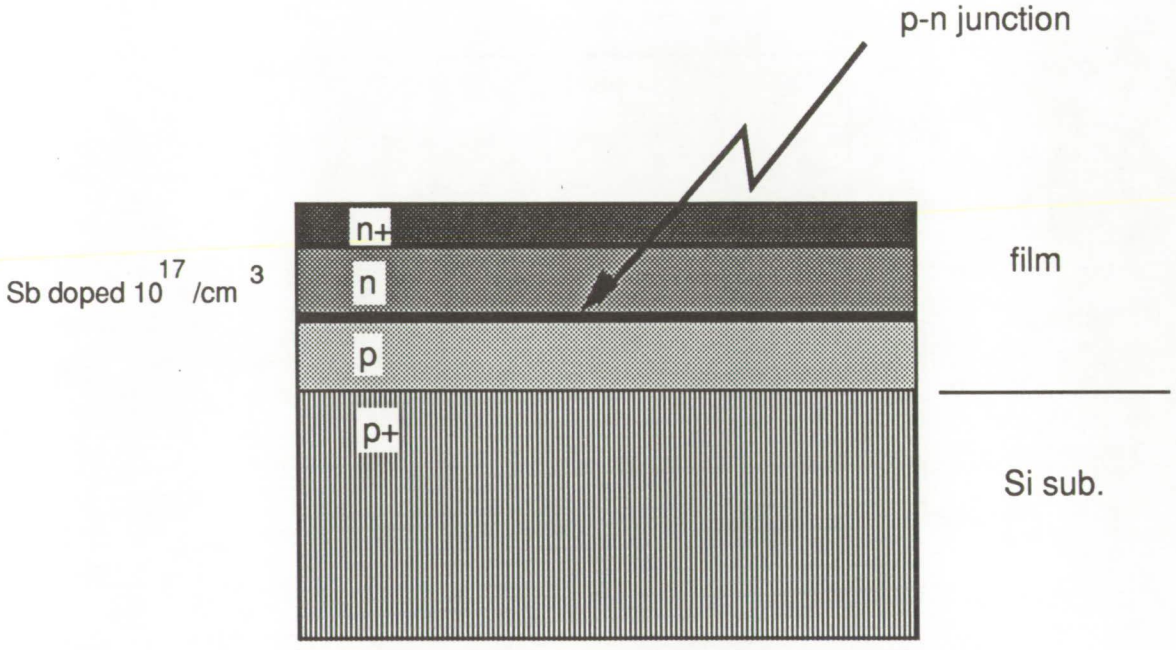


Fig.4.5.5.1. Single MBE grown Si p-n junction layer structure

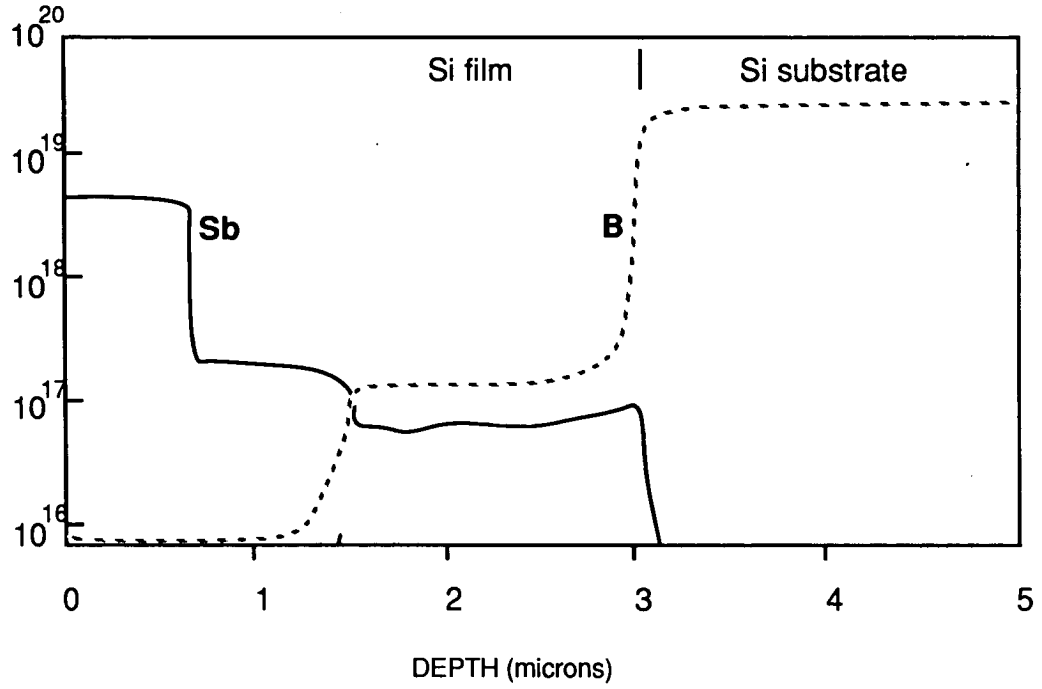


Fig.4.5.5.2 Sb and Boron depth profiles of the Si homo junction grown by MBE

The depth profiles of the MBE grown Si multilayer film doped with B and Sb are shown in Fig. 4.5.5.2. The abrupt changes in B and Sb concentrations were obtained by opening and/or closing respective shutters. The dopant concentrations were controlled by adjusting the corresponding source temperatures. The interface of the p and n layers was clearly defined at the depth about 1.5 micron. The B and Sb concentrations were found to be $5x10^{17}$ atoms/cm^3 and $2x10^{17}$ atoms/cm^3, respectively. Both were slightly higher than the desired values. The B doped epitaxial layer was near 1.5 micron while Sb doped n layer was 0.8 micron. The Sb doped n^+ layer was about 0.65 micron with Sb concentration near $5x10^{18}$ atoms/cm^3.

4.6 Growth of $CoSi_2$ on Si

4.6.1 MBE growth of $CoSi_2$ on Si

We have grown many $CoSi_2$ films on silicon substrates. It optimum growth was as follows. The background pressure of growth chamber was maintained at a low level prior to growth. We have used an UTI residual gas analyzer (RGA) to detect background species and epitaxy in the growth chamber. The RGA spectrum in Fig.4.6.1.1 shows that nitrogen and CO_2 were the dominant background species prior to growth, while Fig.4.6.1.2 reveals the dominant species were Si and Co during growth, as expected. The presence of nitrogen and CO_2 did not appear to influence the $CoSi_2$ epitaxy significantly.

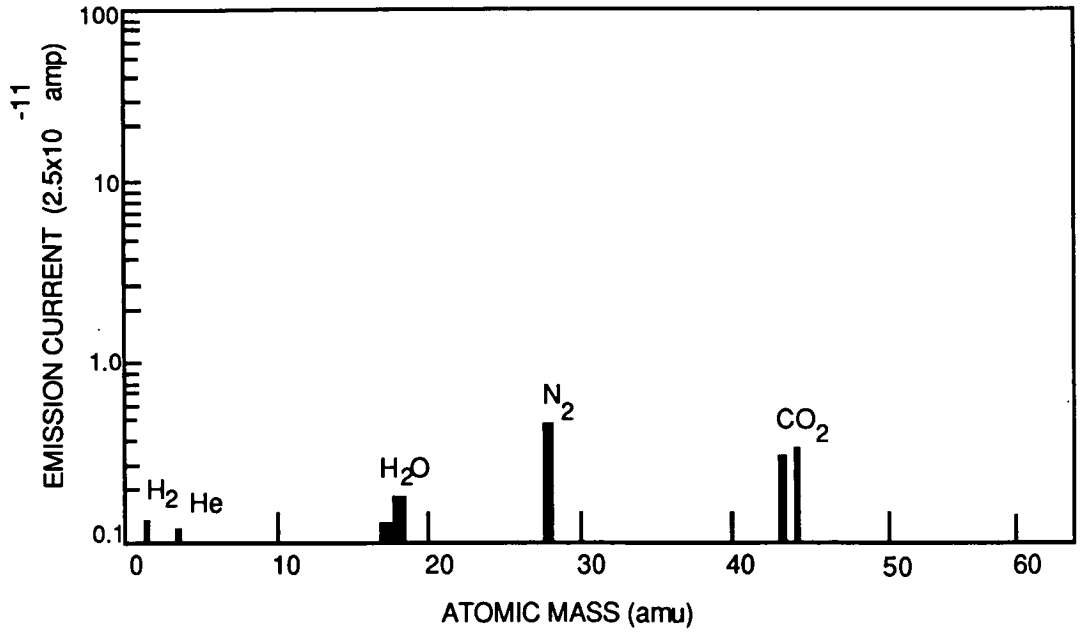


Fig.4.6.1.1. RGA spectrum prior to $CoSi_2$ growth.

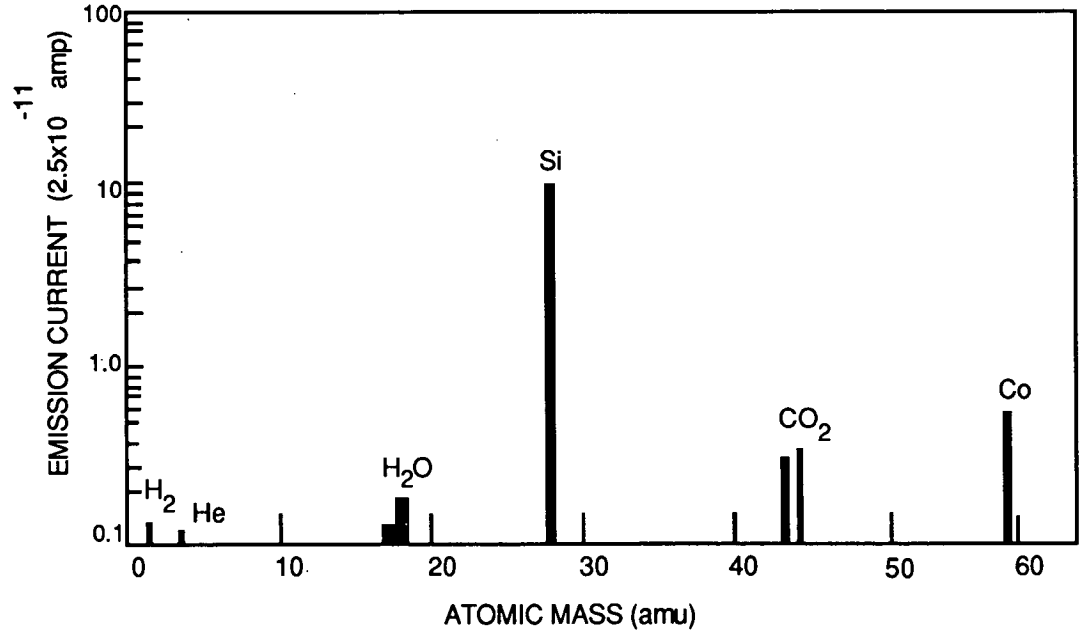


Fig.4.6.1.2. RGA spectrum during $CoSi_2$ growth.

The growth conditions were set prior to growth by adjusting the Si and Co e-beam sources. The substrate temperature was kept at 650°C. The high voltages of the Si and Co sources were 3.3 KV and 4.8 KV, respectively. The filament current was in the range of 10-20 amp. The final thickness was measured with a Tencor alpha-step profiler. We adjusted the emission current rather than the high voltage of e-beam sources to obtain a suitable film thickness and composition. Typically, the emission currents for Si and Co were 164 mA and 200 mA,

respectively. From the measured thickness and the deposition time, we calculated the growth rate. The typical growth rate for $CoSi_2$ was 0.2 μm/hr.

4.6.2 $CoSi_2$ film characterization

We have examined the $CoSi_2$ film crystallinity by X-ray diffraction, enabling us to measure the perpendicular lattice constant of the $CoSi_2$ film. The initial silicon substrate was also measured to check the substrate orientation. The X-ray spectrum of the silicon substrate is shown in Fig. 4.6.2.1. The $CoSi_2$ orientation was found to be the <111> direction.

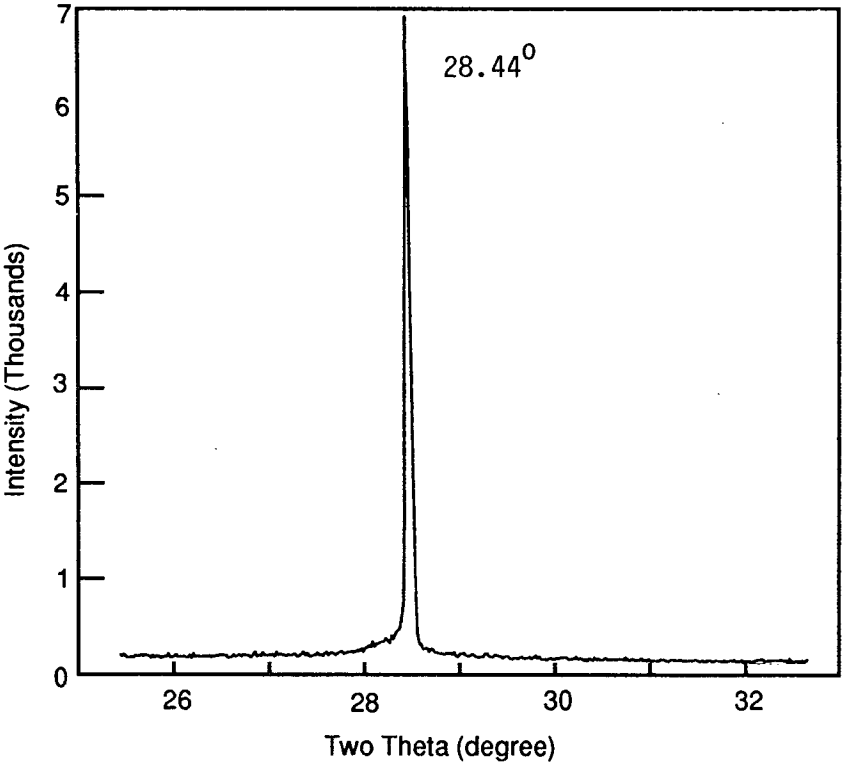


Fig.4.6.2.1. The X-ray spectrum of the silicon substrate showing the <111> orientation.

The X-ray spectrum of a 250Å $CoSi_2$ film is shown in Fig.4.6.2.2. The $CoSi_2$ film was oriented along the <111> direction. We have used the Bragg reflection equation to calculate the lattice constant of the $CoSi_2$ film:

$$2d_{<111>}\sin Q = nl,$$

where $d_{<111>}$is the lattice spacing between (111) planes, l is the X-ray wavelength (1.5405Å) for copper Ka, n equals to 1 for the first order X-ray diffraction. The calculated lattice constant of the $CoSi_2$ film is about 5.363Å.

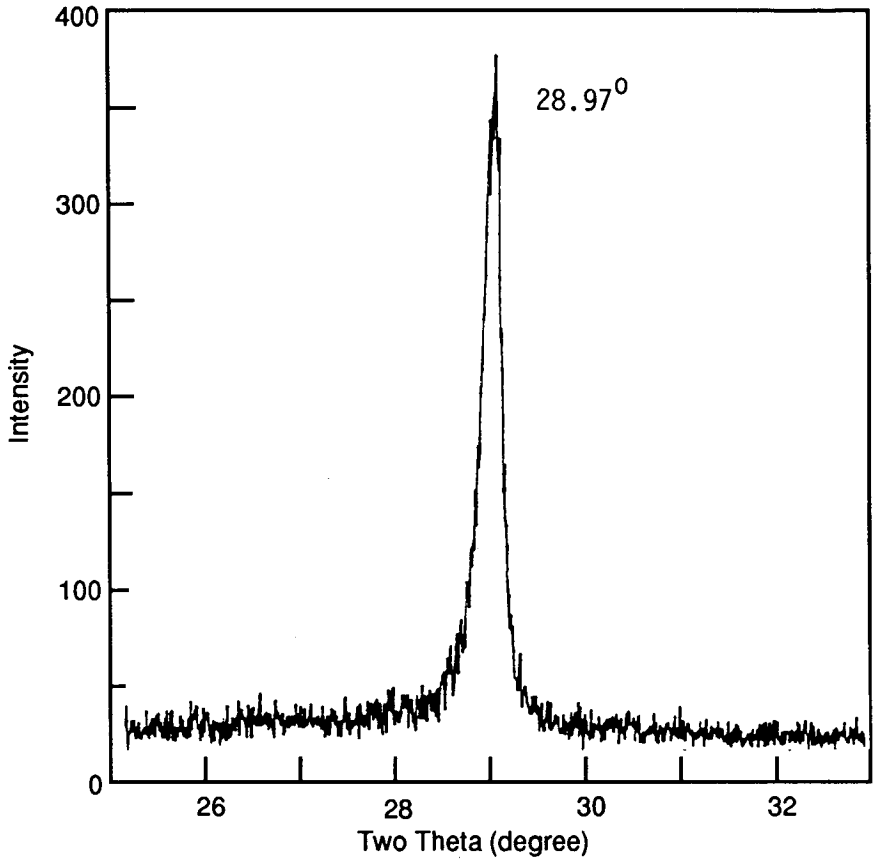


Fig.4.6.2.2. The X-ray spectrum of MBE grown $CoSi_2$ film.

The high crystallinity of $CoSi_2$ film has also been confirmed by Rutherford back reflection spectroscopy (RBS) using a beam of 2.275-MeV He^+ ion. The RBS spectrum shown in Fig.4.6.2.3(a) taken at an incident angle of 160° to the normal surface is generally considered to be a random spectrum and is usually used as a reference, while the spectrum shown in Fig.4.6.2.3(b) taken at normal incidence is called aligned RBS spectrum of our MBE grown $CoSi_2$/Si structure. The spectra show the counts received by each channel of a multi-channel analyzer plotted as a function of the channel number. For this particular case, each channel was 4.3 Kev wide. By multiplying 4.3 Kev by channel number, we could convert the expression to energy for the horizontal axis. The minimum channeling yield c_{min} shown in Fig. 4.6.2.3 is defined as the ratio for the intensity of the backscattered ions from top surface detected along the crystal orientation(<111> in this case) to the intensity of the randomly backscattered ion.

The minimum yield c_{min} at the top surface was estimated to be about 5%. This factor was sensitive to growth conditions such as the substrate temperature and Si/Co flux ratio and hence could be controlled by varying these parameters. The lower the minimum channeling yield the higher was the crystallinity of the film. The aligned yield would thus be near zero for a single crystal film. In other words, the incoming ion beam could travel along the crystal orientation for a long distance without suffering collision to produce a back scatter. The result shown in Fig.4.6.2.3 indicates that the $CoSi_2$ film was of high crystallinity.

In addition to analyzing the crystallinity, RBS was also used for determining the alloy composition and thickness of the grown films. High energy He^+ ions are scattered not only by atoms at the top surface but also by atoms in the bulk. The scattered ion energy from atoms in the bulk is smaller than the energy scattered from atoms at top surface because He^+ ions have lost energy in traveling into the bulk of the sample. Different species and layers of different thickness would result in different scattering energy channels. If the top surface is taken as the origin and x direction is directed from the origin into bulk, as shown in the insert of Fig.4.6.2.3, the actual composition at the surface of the structure could be determined by the ratio of the Si yield to the Co yield at the origin. The first approximation of the atomic concentration ratio is given by

$$C_{Si}/C_{Co} = (Yield_{Si}/Yield_{Co})(Z_{Co}/Z_{Si})^2,$$

where C_{si} ans C_{Co} are atomic concentrations of Si and Co, respectively, and the atomic numbers for Co and Si are Z_{Co} =27 and Z_{Si} =14, respectively. Consider three different Si channel widths of 400-385, 385-375 and 375-355 and three corresponding Co channel widths of 295-280, 280-270 and 270-250, the three corresponding compositions for $CoSi_x$ are $CoSi_2$, $CoSi_6$, and $CoSi_3$. The average Co yield was 7310 in channel 400-385 and 4328 in channel width 295-280 for Si. From the above equation, the composition ratio C_{Si}/C_{Co} turned out to be 2. Fig.4.6.2.4 shows a composition profile of the $CoSi_2$/Si sample.

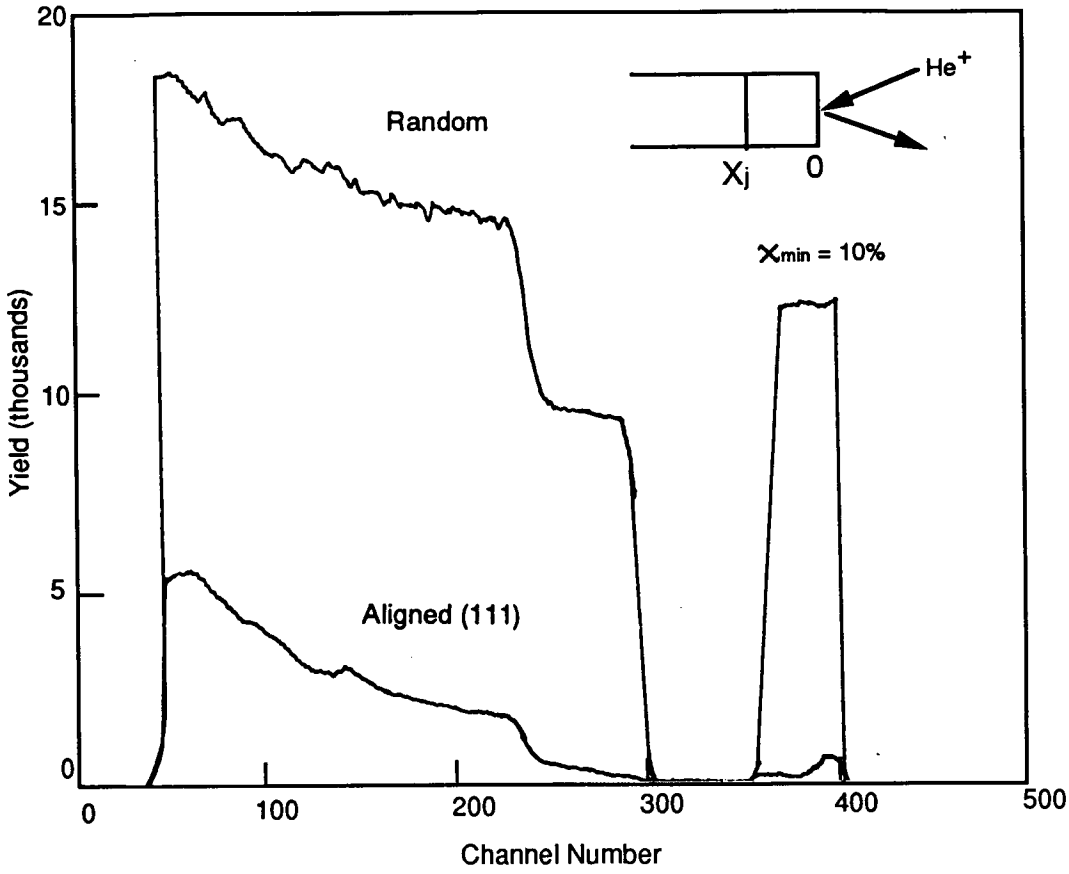


Fig.4.6.2.3. RBS spectrum taken at 160 ° to normal direction for MBE grown $CoSi_2$

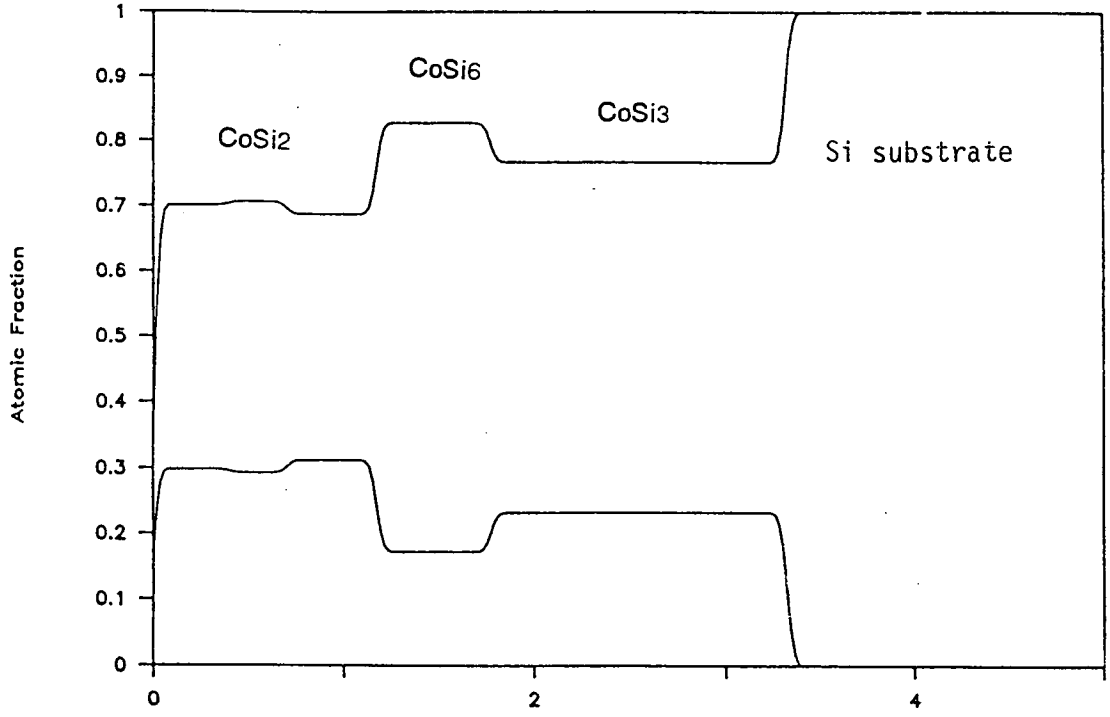


Fig.4.6.2.4. Composition depth profile of the $CoSi_2$ film.

We have also studied the interdiffusion of Co and Si at high temperatures because the melting point of $CoSi_2$ is low (~1195°C). We have to prevent $CoSi_2$ from diffusing into p-n junctions because the formation of a stack of p-n junctions was carried out at relatively high temperatures. The MBE grown $CoSi_2$ sample was annealed at 800°C for 5 hours in-situ in the growth chamber. The $CoSi_2$ sample was characterized by RBS. The RBS spectra of the Co signal are shown in Fig.4.6.2.5. The results show that Co composition changed very little after the high-temperature annealing, indicating the high-temperature stability of the MBE-grown $CoSi_2$ films over a prolonged period of high-temperature growth condition. This stability allowed us to perform a subsequent high-temperature growth of another p-n junction on top of the silicide without damaging it or causing unacceptable interdiffusion within the $CoSi_2$/Si structure.

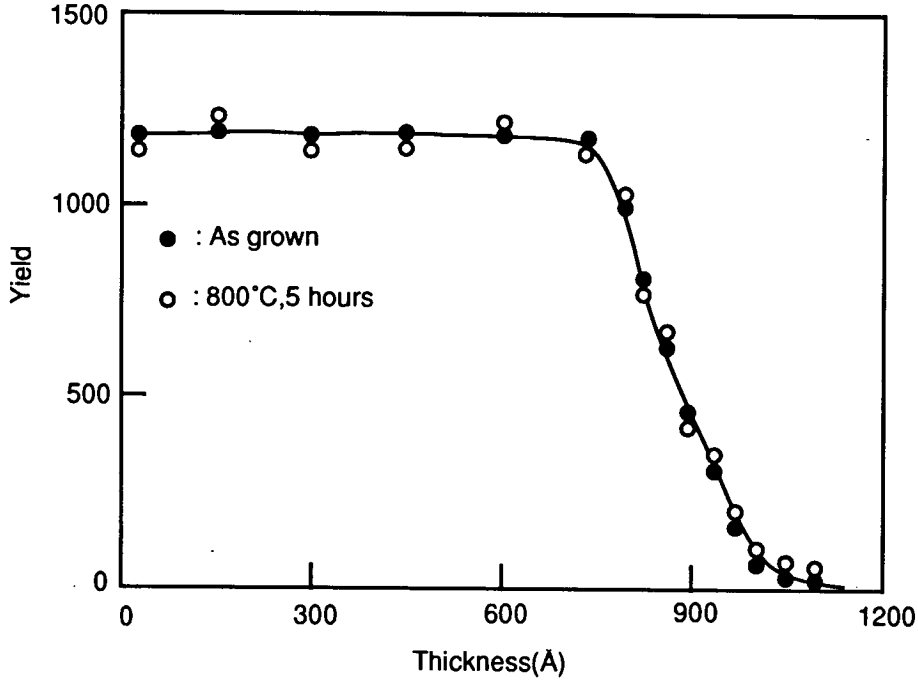


Fig.4.6.2.5. Random RBS spectra of the Co profiles of a 800Å thick $CoSi_2$ film before and after thermal annealing (800°C for 5 hours).

A most welcome result was that all the $CoSi_2$ films grown by MBE or by SPE under the low-growth rate described above were free of pinholes, revealed by microscopic, etching and RBS examinations. This was a very important result because it meant that the $CoSi_2$ layers were of very high quality, better than the stat-of-the-art, and that uniform growth of the $CoSi_2$/pn-junction combination over a large surface area of the wafer substrate was also possible. We

attributed the pinhole-free quality to the low growth temperature and rate and the thin layers grown.

4.6.3 Resistivity measurement of the $CoSi_2$ films

We have measured the resistivity of the $CoSi_x$ films as a function of the composition x. The sheet resistance was measured by a four-point probe. The resistivity was calculated as the product of sheet resistance and film thickness assuming the film concentration was uniform. As shown in Fig.4.6.3.1, the resistivity of the $CoSi_x$ film increased with increasing composition x. It turned out that the resistivity of our as-grown $CoSi_x$ (x=2) without annealing was considerably lower than the required 10^{-3} Ohm-cm, ideal for good interconnection between p-n junctions.

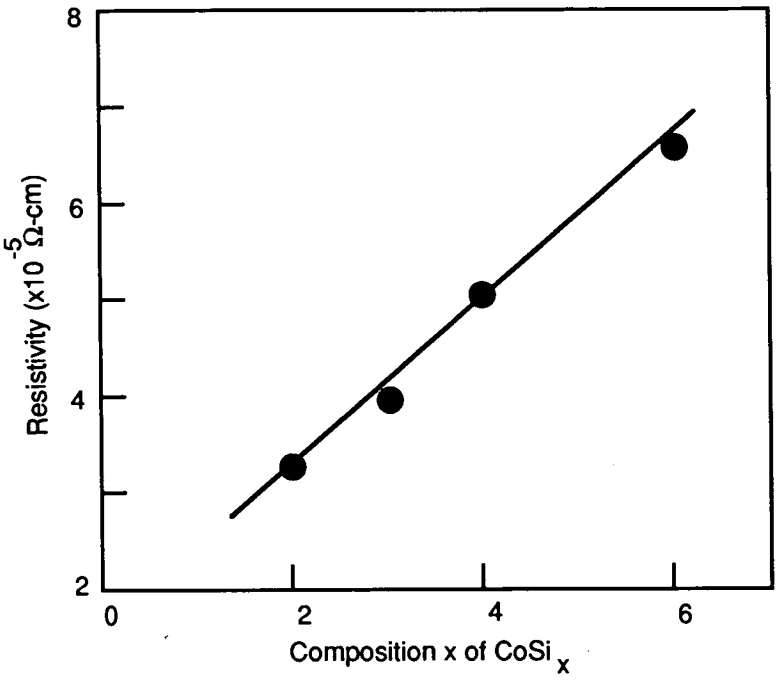


Fig.4.6.3.1. The resistivity of $CoSi_x$ films as a function of the composition x.

4.6.4 Solid phase epitaxy (SPE) of $CoSi_2$ on Si p-n junction

We have also performed $CoSi_2$ growth on Si p-n junction by the solid state epitaxy (SPE) method using 1/2"-diameter rod-fed e-beam sources. The p-n junction was formed on a Si n/n^+ <100> 3"-diameter wafer. The SPE growth was made by first depositing a Co metal layer on the Si wafer, and then annealing this layer at a high temperature so that the Co diffused into and reacted with the Si to form the $CoSi_2$. The growth rate of SPE-$CoSi_2$, starting with a deposit of a thick Co layer on the Si, was a non-linear function of the annealing time within the annealing temperature range of 600 °C to 800 °C, as shown in Fig.4.6.4.1. If the Co film

was thin (<1000Å) and the annealing time was long, the thickness of $CoSi_2$ produced would be limited by the available Co material in the deposited Co film. A 50-Å thick Co film produced a 150 Å-thick $CoSi_2$ layer. This thickness was sufficient for low-resistivity connections.

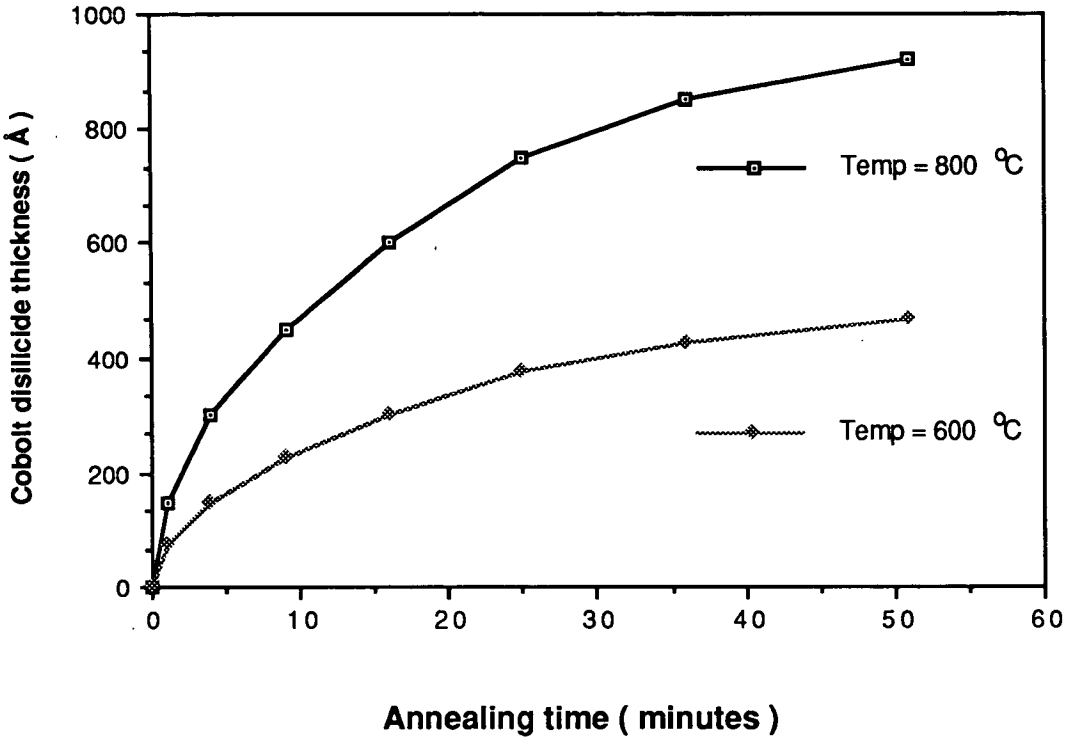


Fig.4.6.4.1. SPE grown $CoSi_2$ thickness vs. annealing time.

While the thickness of MBE-$CoSi_2$ could be directly measured by the Tencor stepper, the thickness of SPE-$CoSi_2$ had to be inferred indirectly from measured data of spreading resistance profile and I-V/etching depth data. Spreading resistance method was carried out by lapping the Si chip at an angle of about 6° from the top surface. A two-point probe measured the resistivity along the lapped surface. Typically, the resistivity of $CoSi_2$ film was very low compared with p-n junction. If the distance of the two-point probe was L, the thickness of the $CoSi_2$ film was L x sin 6° = 0.1045 L. More accurate resistivity measurement was also made by measuring resistance on the $CoSi_2$ layer while it was being delineated by a chemical etch. A chip was cut to about 2mm x 5 mm from the wafer containing the $CoSi_2$ film, and two probes attached to the two ends of the slab were used to measure the $CoSi_2$ resistivity while a chemical etching ink was applied on the middle of the slab to etch $CoSi_2$ film. The etching solution used was a solution of HF, HNO_3, CH_3COOH and H_2O. The ratio of HF: HNO_3: CH_3COOH: H_2O was 5:3:3:24 and the etching rate was about 10 Å/s. As soon as an abrupt change in

resistivity occurred, the etch was stopped and the abrupt change in resistivity indicated that the $CoSi_2$ film was just etched through, as shown in Fig.4.6.4.2. The etched depth was then measured by the Tencor stepper. The sheet resistance of $CoSi_2$ was measured by the 4-point probe method, from which the resistivity was calculated as the product of sheet resistance and the $CoSi_2$ thickness. The advantages of SPE-grown $CoSi_2$ were that its growth required only a single Co source and that its thickness was automatically produced by a self-stop process, determined by consumption of the Co layer during annealing. In contrast, the main advantages of MBE-grown $CoSi_2$ were that the Co/Si flux ratio could be independently controlled and that there was no film thickness limitation. The detailed SPE growth procedure developed is as follows:

(1) Clean a Si p-n junction substrate by Si flux at 800 °C for 30 minutes in UHV.

(2) Cool down substrate to room temperature.

(3) Turn on Co e-beam source to deposit 50 Å Co film

(4) Raise substrate temperature to 600 °C for 20 minutes.

(5) Continue to next material growth if necessary.

4.6.5 Quality of $CoSi_2$ on Si p-n junction

All grown $CoSi_2$ films were evaluated by RBS for crystallinity and by four-point probe test for resistivity. Both SPE-grown and MBE-grown films showed excellent crystallinity, revealed by the low minimum channeling yield c_{min} ($\approx$ 5%) of the RBS spectra, and low resistivity ($< 10^{-3}$ Ohm-cm) meeting the high-efficiency converter requirement. The RBS spectrum of the SPE-grown $CoSi_2$ is shown in Fig.4.6.5.1, showing the crystallinity of $CoSi_2$ film as good as that of the MBE-grown film The temperature dependence of resistivity of the SPE-grown and MBE-grown films is shown in Fig.4.6.5.2, showing that the resistivity of MBE-grown films increased more sharply with increase in temperature in the 100 - 400K range than the SPE-grown films. This behavior is important for the construction of high-efficiency converter: as the SPE films appeared to be a better choice for interconnection between the p-n junctions, and their fabrication was more straightforward, they would be more amenable to mass production.

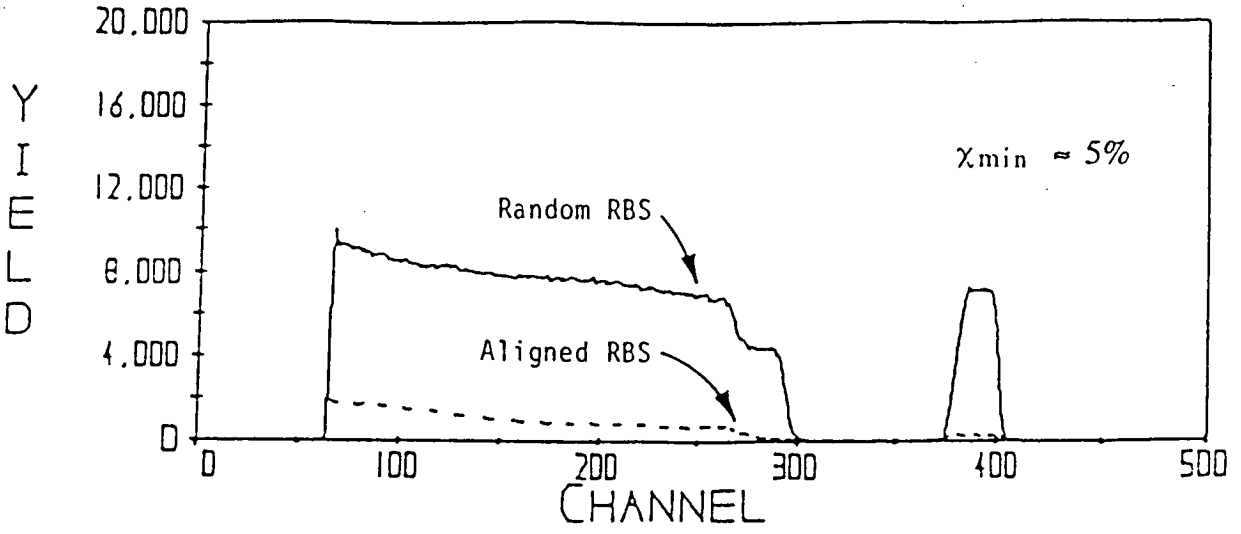
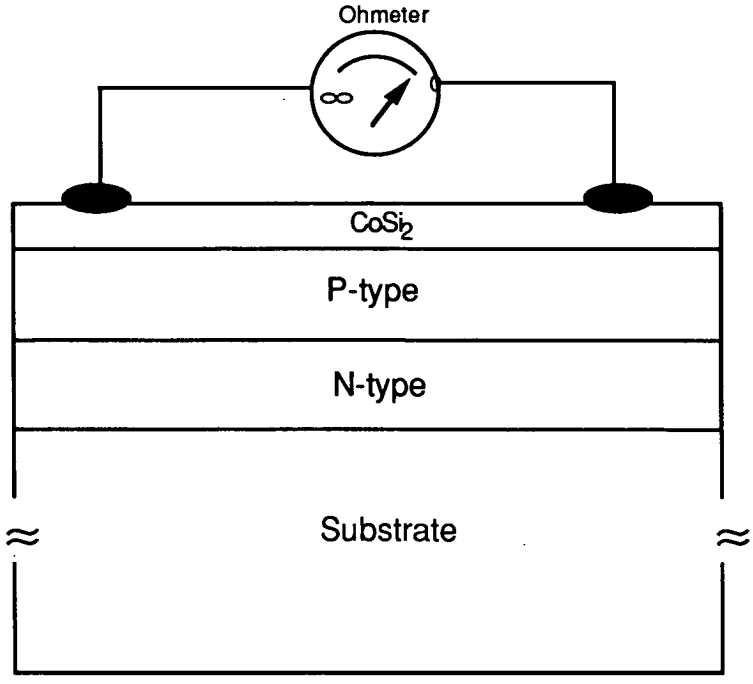
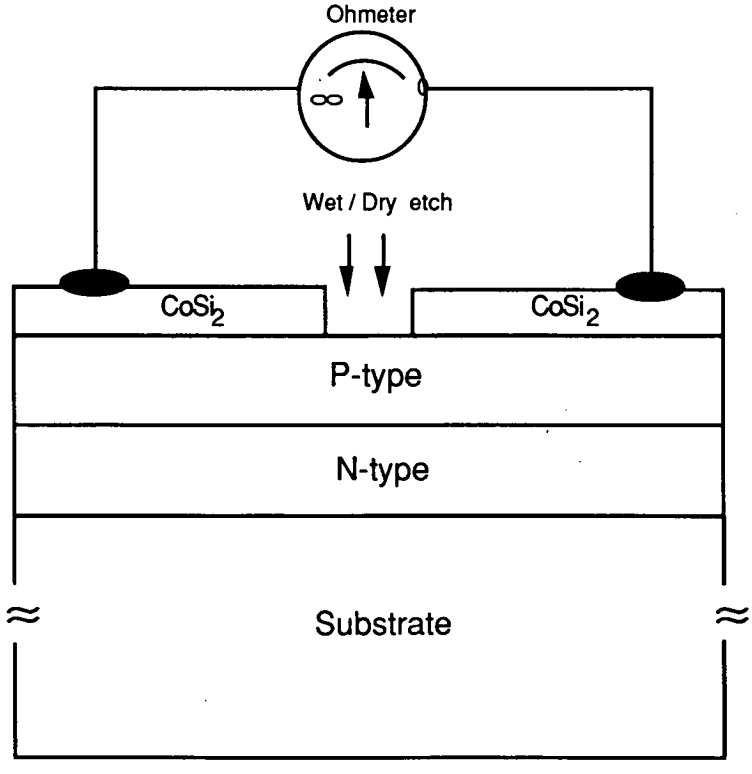


Fig.4.6.5.1. RBS spectrum of SPE $CoSi_2$ film grown on Si p-n junction.



(a) An Ohmeter is connected to both ends of a chip during etching process.



(b) Resistance goes higher as soon as $CoSi_2$ film is etched through.

Fig. 4.6.5.2. Method of measuring resistivity of the silicide film accurately.

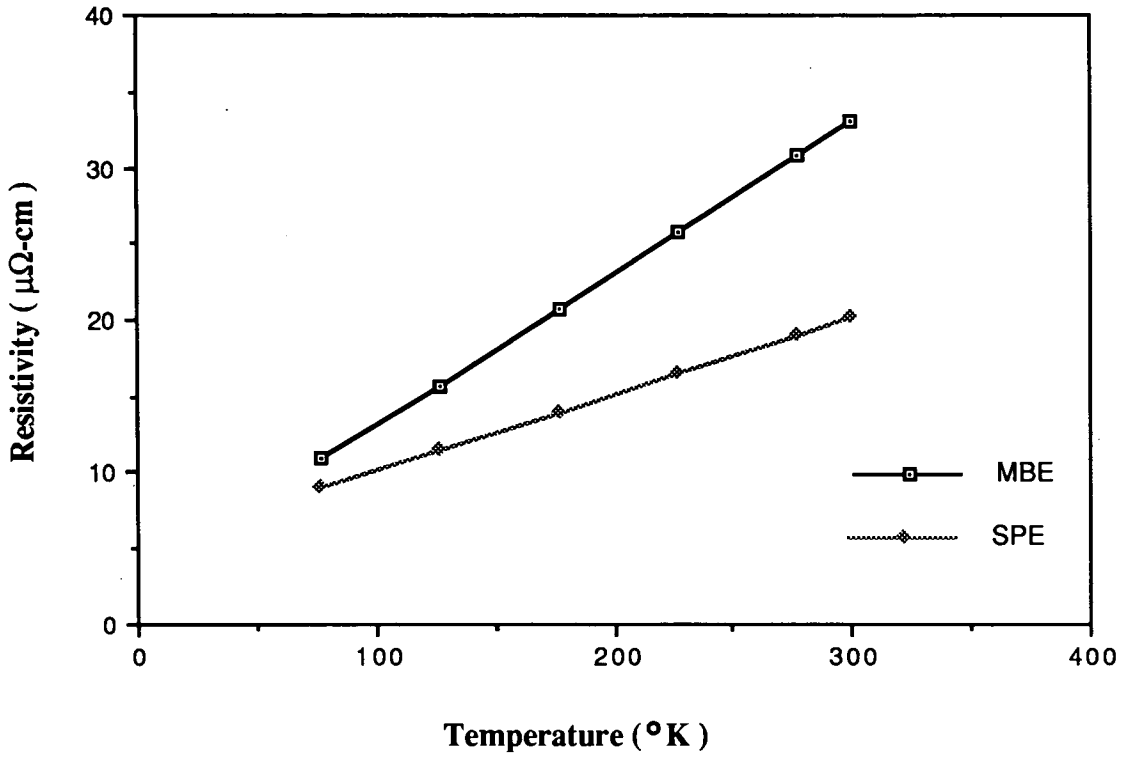


Fig.4.6.5.3. Resistivity of $CoSi_2$ films as the function of temperature.

4.7 MBE growth of Si on $CoSi_2$ stacked on Si p-n junction

Having successfully grown high-quality $CoSi_2$ films on Si p-n junction, we now tackled the epitaxy of Si on a $CoSi_2$ layer. We have found that the optimum growth temperature for epitaxy of Si on $CoSi_2$ was about 600 °C, and the optimum Si growth rate was about 1 micron per hour. The RBS spectra of the Si film are those shown in the Fig.4.7.1 and 4.7.2. Both MBE-grown and SPE-grown $CoSi_2$ were used for this experiment. The thickness of both the MBE-grown and SPE-grown $CoSi_2$ was about 200 Å. The thicknesses of Si films grown on MBE-$CoSi_2$ and SPE-$CoSi_2$ were 500 Å and 2000 Å , respectively. Both Si films produced a channel yield c_{min} of about 10% (in contrast to the 5% for Si on Si), indicating that the crystallinity of the Si film on $CoSi_2$ was not as good as the Si grown on Si or on p-n junction. This lowering of crystallinity was still acceptable for converter fabrication, provided that no progressive degradation occurred, and that the number of p-n junctions per stack was small, say 10.

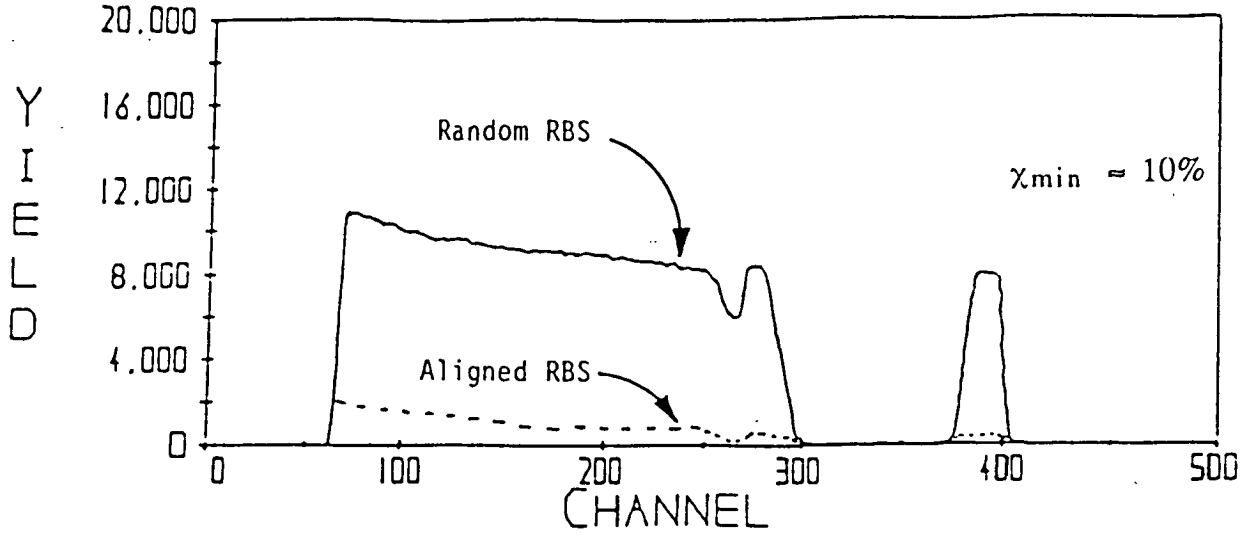


Fig.4.7.1. RBS spectrum of MBE-grown Si on SPE-grown $CoSi_2$ layer on top of a Si p-n junction.

Fig.4.7.2. RBS spectrum of MBE-grown Si on MBE-grown $CoSi_2$ layer on top of a Si p-n junction.

4.8 Growth of double p-n junction with $CoSi_2$ interconnection

Our next experiment was the growth of two p-n junctions connected in series by a SPE-grown $CoSi_2$ layer forming a small stack of p-n junctions. SPE-$CoSi_2$ layer was chosen because it has a higher conductivity. The growth process developed is as follows:

(1) Clean a Si wafer and load into MBE chamber.

(2) Perform Si flux cleaning at 800 °C substrate temperature for 30 minutes.

(3) Reduce temperature to 650 °C

(4) Turn on Si e-beam source and open the shutter of B for 5 hours. The Si growth rate is 0.2 m/hr and the B temperature is 1000 °C.

(5) Cool down substrate to room temperature.

(6) Deposit 50 Å Co by e-beam source at the growth rate of 100 Å/min.

(7) Anneal the substrate at 650 °C for one hour.

(8) Turn on Si source again and open the shutter of Sb for 5 hours.

(9) Grow p-type (B dopant) Si for 5 hours.

(10) Turn off e-beam source and close B shutter after final p-type growth.

On evaluation of the double p-n junction structure by RBS, the B dopant was found to have reacted with the SPE-$CoSi_2$ when annealed at 800 °C, penetrating deep into the SPE-$CoSi_2$ and n-type region, as shown in Fig.4.8.1, showing the contrasting B profiles for the SPE-$CoSi_2$ annealed at 650 and 800°C. The Sb dopant did not react with the SPE-$CoSi_2$, as shown in Fig.4.8.2, showing the respective B, Sb and $CoSi_2$ profiles for the SPE-$CoSi_2$ film annealed at 650°C rather than 800°C. The problem of B diffusion was solved by reducing the SPE-$CoSi_2$ annealing temperature from 800 to 650 °C.

Due to the low growth rates, we have run out time and resources to fabricate more than three p-junctions in series, and therefore the fabrication of a stack of a large number of p-n junctions could not be carried out at this time. However, the RBS results and the MBE techniques that

we have developed thus far showed that the developed procedure is capable of constructing the multiple p-n junction in tandem.

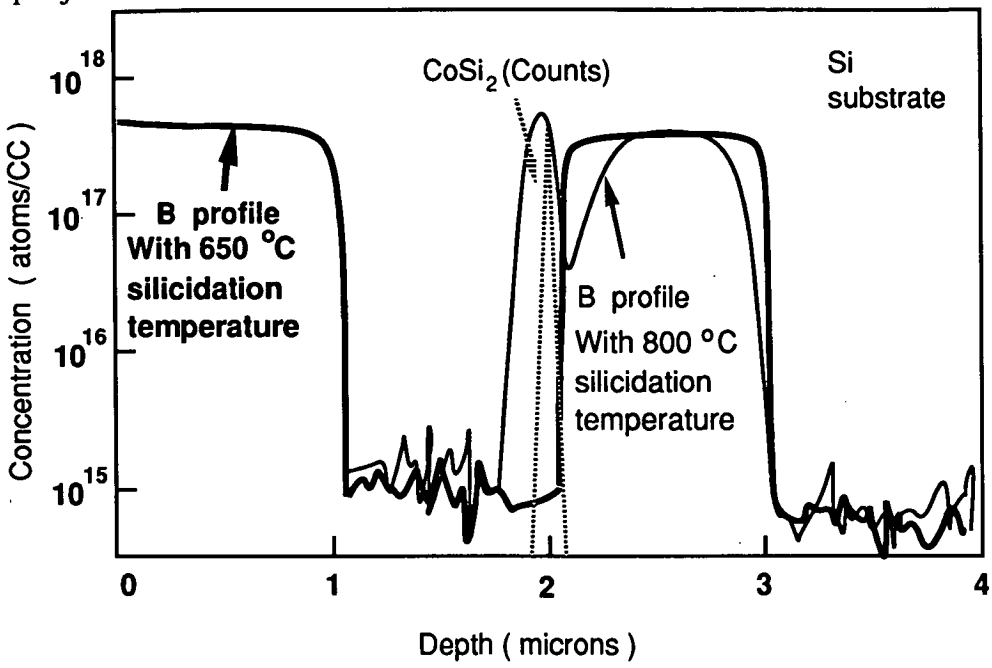


Fig.4.8.1. SIMS profiles for B in a double p-n junction with a SPE-$CoSi_2$ interconnecting layer annealed at 650 °C and 800 °C. When annealed at 800°C the B penetrated the $CoSi_2$ and n region.

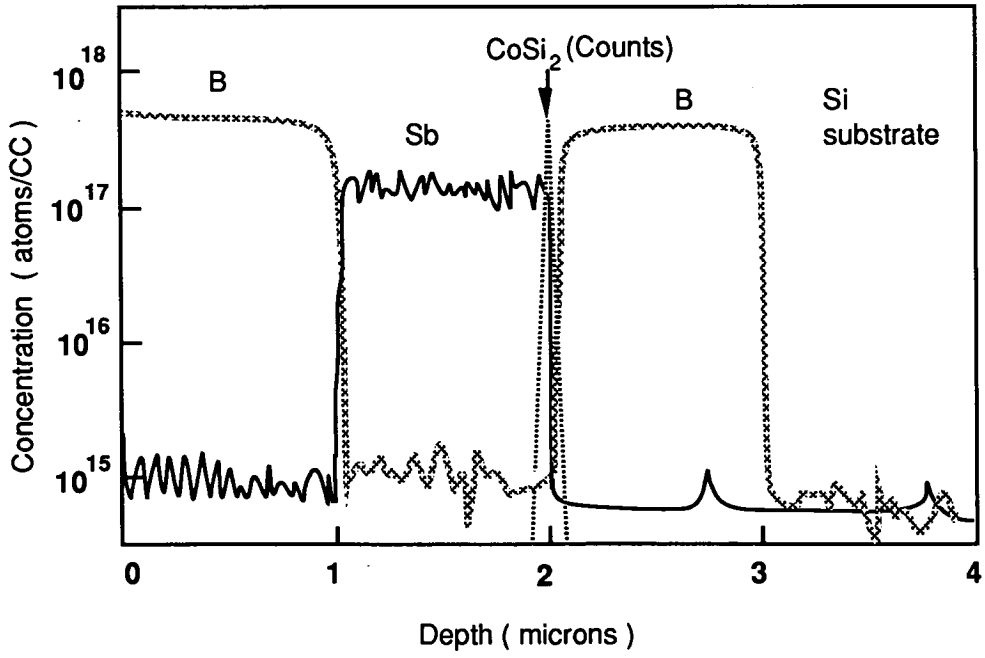


Fig.4.8.2. SIMS profiles for B and Sb in a double p-n junction with SPE-$CoSi_2$ interconnection annealed at 650°C.

5.0 DEVICE CHARACTERIZATION

5.1 Devices Preparation

To characterize photovoltaic behaviors of the p-n junctions and double p-n junctions fabricated in this program, we have delineated the grown films into small mesa structures. The typical linear dimensions of these mesas ranged from 50 to 500 microns. The recipe used to delineate the mesa is as follows:

1. Clean the Si sample surface with acetone, rinse with DI water and then blow dry with N_2 if necessary.

2. Apply a thin layer of positive Microposit Photo Resist (PR) material (1400-31: 1400-17 = 1:1) to the surface of the Si sample using spin-on method.

3. Bake the PR-coated Si sample at 90 °C for 30-40 minutes.

4. Cover the PR-coated Si surface with a mask of desired pattern.

5. Expose the PR coating through the mask to UV light.

6. Develop the PR coating with Microposit MF-319 solution, rinse with DI water and blow dry with N_2.

7. Bake the developed PR coated Si sample at 125 °C for (30-40) minutes.

8. Etch the Si sample with CP-4A solution ($HF:HNO_3:CH_3COOH$ = 3:5:3, 35 micron/min) for suitable time and rinse with DI water thoroughly.

9. Remove the PR coating using acetone, rinse with DI water and blow dry with N_2.

5.2 I-V characterization of single Si p-n junction

The I-V curve of the MBE-grown p-n junction was measured with a Textronix 575 transistor curve tracer. The probing arrangement is shown in Fig. 5.2.1. The electrical contacts to individual junctions were made by pressing a spring-held sharp needle on the top surface of delineated Si diode and another needle to the metal base plate. A microscope was used to assist precision probing.

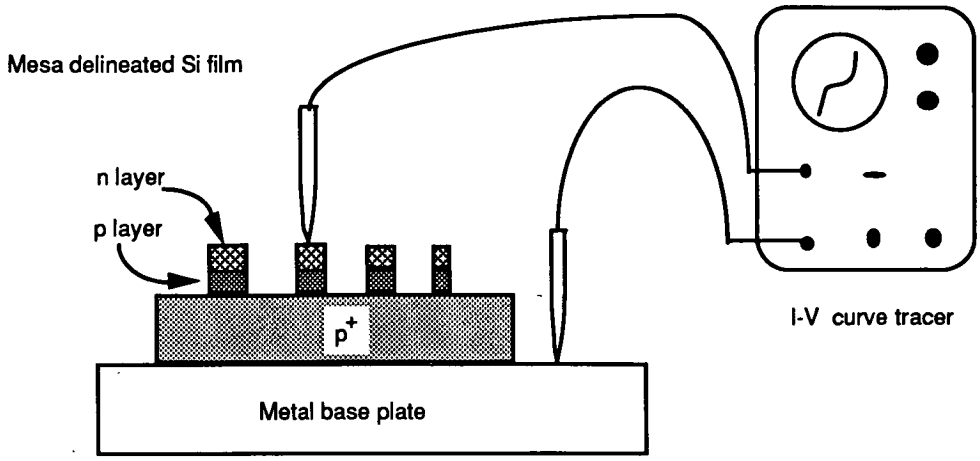


Fig. 5.2.1. I-V curve probing test setup.

Two types of diodes were fabricated and tested: (a) n (Sb-doped) on p-substrate, and n(Sb-doped)-p(B-doped) on p-substrate. The type (a) diodes always showed a higher breakdown voltage, as shown in Fig. 5.2.2. We found that, in the reverse bias condition, the break down voltages were rather sharp in the two types of diodes. The typical breakdown voltage ranged from 30 to 40V for (a) diodes and 10 to 15 volts (b) diodes. Since the p-n junction was abrupt for both diodes, the carrier concentration of the lightly-doped side of the junction could be estimated, if avalanche breakdown mechanism was assumed. We found the carrier concentration of the light doping side to be $2x10^{16}$ atoms/cm^3 for (a) type and $2x10^{17}$ atoms/cm^3 for (b) type.. These were in good agreement with the boron doping concentration in the p-layer measured by SIMS. The leakage current before breakdown was found to be less than $1x10^{-6}$ amps. The cut-in voltage was found to be 0.5-0.6 V. The dynamic resistance estimated from the I-V curve was about 500 Ω. This could be due to poor contact between the needle tip and the surface of Si p-n junction. No special effort has been made to make good ohmic contacts.

5.3. I-V characteristics of multiple p-n junction structure

The I-V curve of a single p-n junction is shown in Fig.5.3.1(a). The cut-in voltage was about 0.4V and the breakdown voltage was about 100V. The I-V curve shown in Fig.5.3.1(b) is for two p-n junctions connected in series by an external wire. The cut-in and breakdown voltages were double that of the single p-n junction. The I-V curve shown in Fig.5.3.1(c) is for a two p-n junctions fabricated by MBE and connected internally by a SPE-$CoSi_2$ layer. The breakdown voltage of this device was about the same as the single p-n junction. The photodiode V_{oc} was proportional to p-n junction built-in voltage (V_{bi}) given by:

$$V_{bi} = \frac{k_b T}{q} \cdot \ln\left(\frac{N_D N_A}{n_i^2}\right) \sim V_{oc} \qquad (5.1)$$

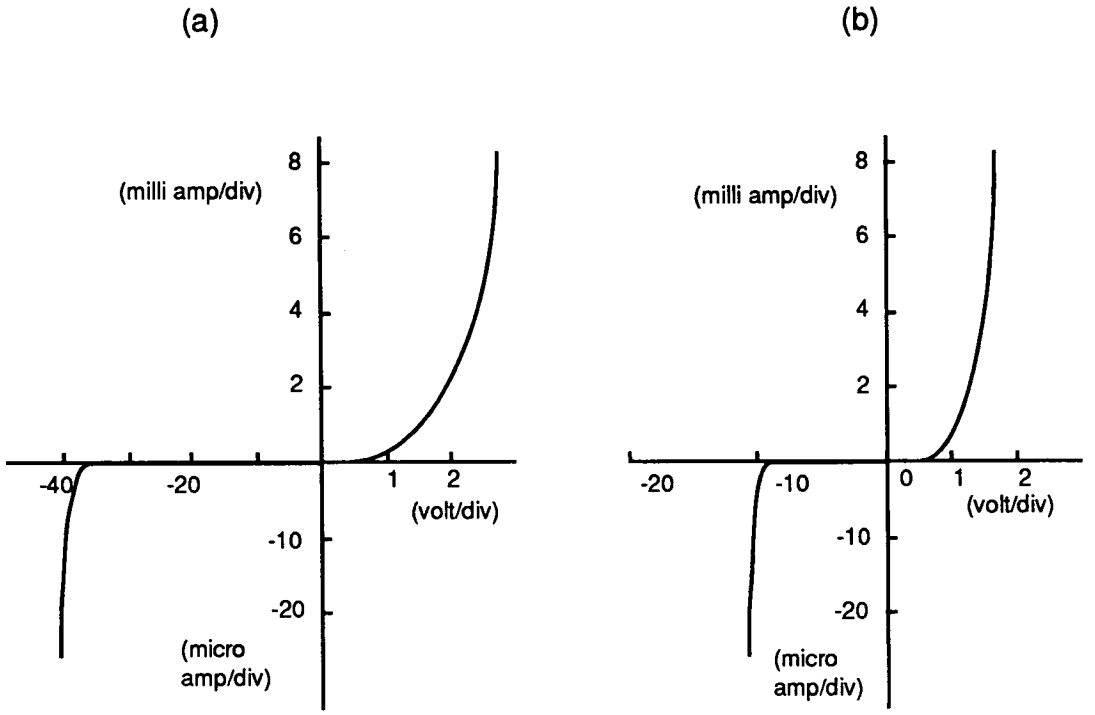
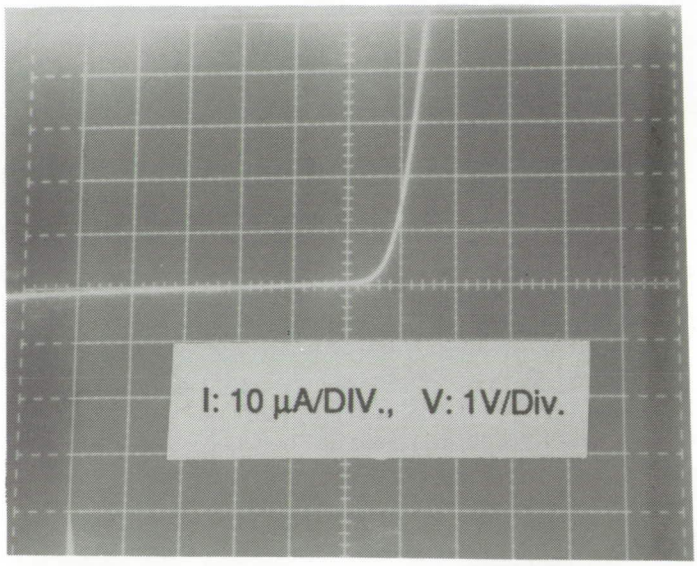
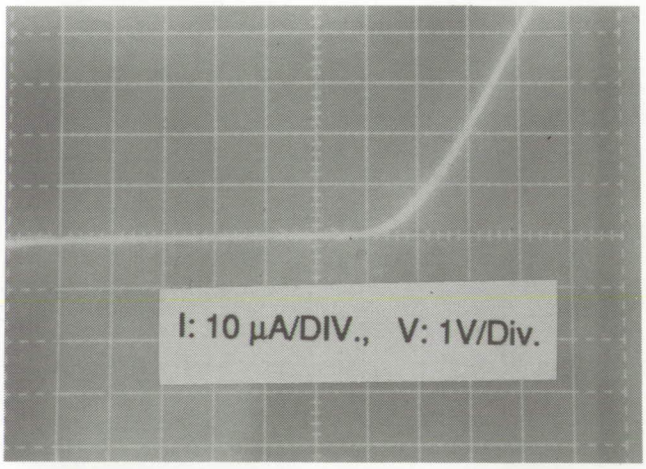


Fig.5.2.2. I-V curve of the Si diodes fabricated by MBE: (a) n (Sb-doped Si) on p-substrate and (b) n (Sb-doped)-p (B-doped) on p-substrate.

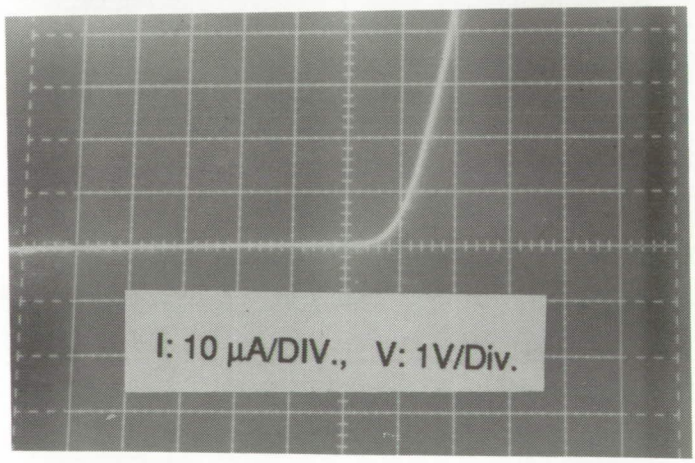
The V_{oc} for device (a) was about 0.4V and about 0.8V for devices (b) and (c). In the device having the two junctions connected together externally, the V_{oc} was doubled as expected. The major difference between device (b) and (c) was the serial resistance. The series resistance for devices (a) and (c) was about the same, 500 Ohm, which was the inverse of the slope in the forward-bias curve. This means that the series resistance of device (c) did not increase when it was fabricated from the device (a) configuration, clearly revealing that the $CoSi_2$ layer contributed little to the series resistance. The 500-Ohm series resistance measured was probably due to the contact resistance of the silver paste used, and was not related to the internal series resistance, negligible by comparison.



(a). I-V curve for a single p-n junction.



(b). I-V curve for two p-n junctions connected in series externally by a wire.



(c). I-V curve for two p-n junctions connected in series internally by a $CoSi_2$ layer..

Fig. 5.3.1. I-V characteristics of multiple junctions.

5.4 Optical response

A simple optical response test setup, shown in Fig. 5.4.1, was used to provide qualitative photoresponse test of the MBE-fabricated devices. The test device was delineated and mounted on a pc board. Evaporated Al contact was to the frontside of the device for ohmic contact, and evaporated Al/Ti contact was made to the backside, n^+-substrate. An antireflection (AR) of SiO was evaporated onto the device, and it also acted as passivation coating. A 60-W lamp seated on the travelling-bar of an optical beach was used as a light source. A curve tracer was used to measure the device's optical response. The device and the optical source were shielded in a dark chamber.

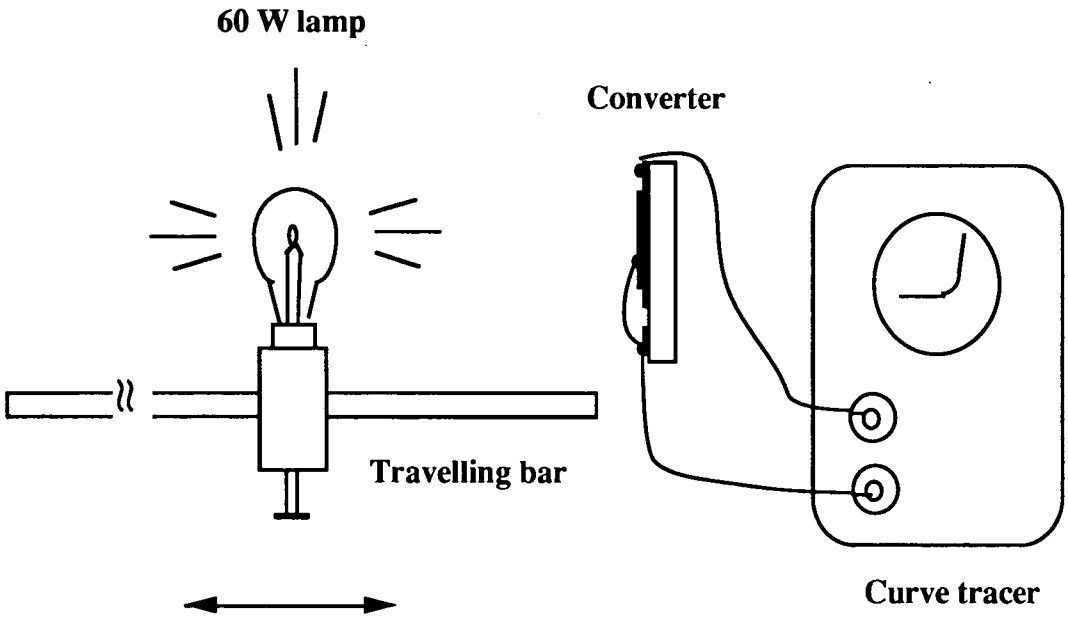


Fig. 5.4.1. The experiment set-up for measuring optical response.

The value of V_{oc} and I_{sc} were measured by the curve tracer and used to calculate the output electrical power. By altering the distance between the light source and the device, the dependence of the electrical output power and the light intensity could be estimated to provide a qualitative measure of the photoresponse of the device, as shown in Fig.5.4.2. More quantitative measurements to verify the device's practicality with a laser source could not be made at this time because our devices did not contain sufficient p-n junction layers to accommodate the size of a laser beam

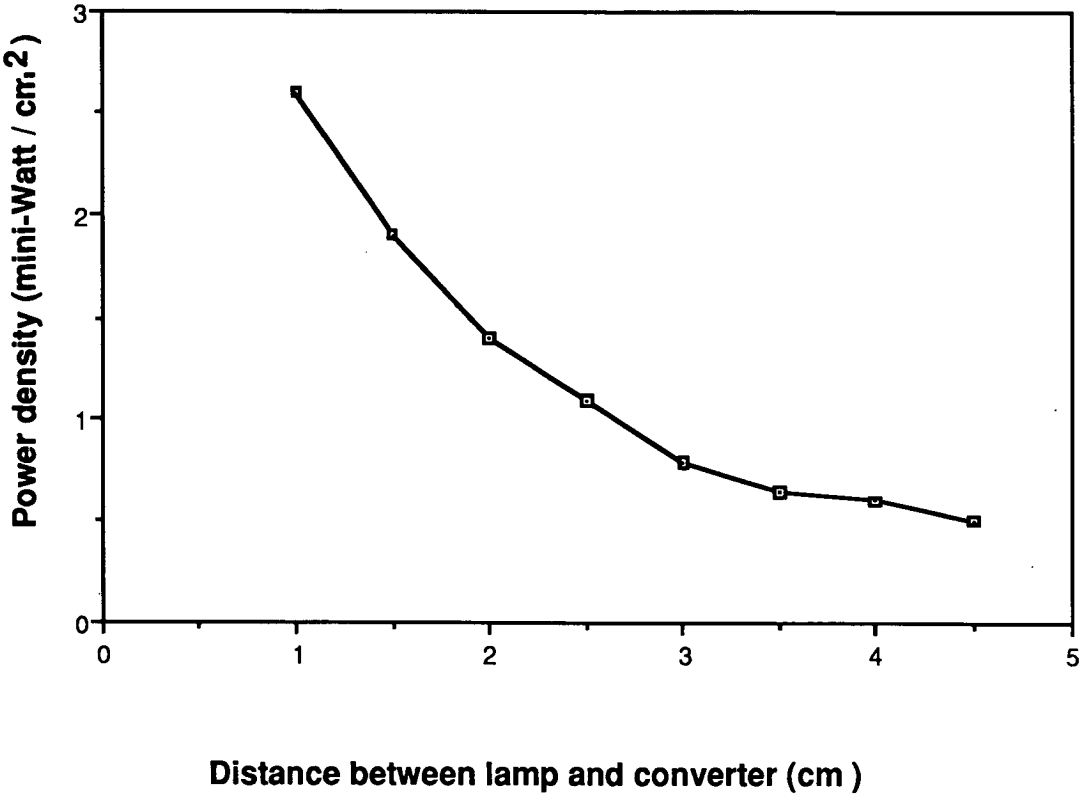


Fig.5.4.2. Distance dependence of output electrical power density.

6.0 CONVERSION EFFICIENCY IMPROVEMENT

6.1 Efficiency

The converson efficiency of the laser converter is defined as the ratio of the maximum output electrical power to the incident laser power:

$$\eta = \frac{I_m V_m}{P_{in}} \sim \frac{I_{sc} V_{oc}}{P_{in}}$$

where P_{in} is the incident laser power, I_{sc} is the short circuit current and V_{oc} is the open circuit voltage of the converter. To increase conversion efficiency with the same input power, I_{sc} and V_{oc} must be increased by making the best of the incident power and reducing the ohmic loss in the converter.

In this effort we have concentrated on perfecting the multilayer growth and optimizing the low-resistivity $CoSi_2$ layers to achieve high conversion efficiency. However, to ensure achieving the 50% conversion efficiency predicted by Walker et al.,[2] the following improvements should also be made: application of an antireflection coating, reducing the surface recombination at interfaces and increasing the number of p-n junctions. These are discussed below.

6.2 AR Coating

After perfecting the multiple p-n junctions, the application of an anti-reflection coating to the vertical junctions will improve the converter efficiency.[12] Made by evaporation, this coating produces a minimum reflectivity when the phase angle, ϕ, of the optical coating should be $\pi/2$ corresponding to odd multiples of $\lambda_0/4$, where λ_0 is the mid-band wavelength of the incident radiation. This phase angle is related the coating thickness and refractive index:

$$\text{Sin } \phi = 2\pi n_1 d_1 / \lambda \qquad (6.1)$$

where n_1 is the refractive index of the coating, d_1 is its thickness, n_2 is the refractive index of the underlying Si, n_0 is refractive index of air and λ is the wavelength of incident laser beam. Then, at the minimum reflectivity condition the minimum reflectivity is given by:

$$R_{min} = \left[\frac{n_1^2 - n_0 n_2}{n_1^2 + n_0 n_2} \right]^2 \qquad (6.2)$$

and is equal to zero if $n_1^2 = n_0 n_2$. In our case, $n_0 = 1$ for air and $n_2 = 3.5$ in the wavelength range of 1.0-1.1 micron for the Si substrate. The best index for the coating is equal to $\sqrt{n_{Si}}$, which is equal to 1.87. We have chosen SiO because it has an index of 1.8-1.9, and it can be evaporated easily by using Tungsten filament heating.

To complement the AR coating and to reduce the reflectivity even further, the surface of the vertical junctions should be roughened by lapping or fast etching, as illustrated in Fig. 6.2.1, showing the modeled reflectivity of a roughened surface contrasting with that of the flat surface. Clearly the roughened surface is better for all wavelengths.

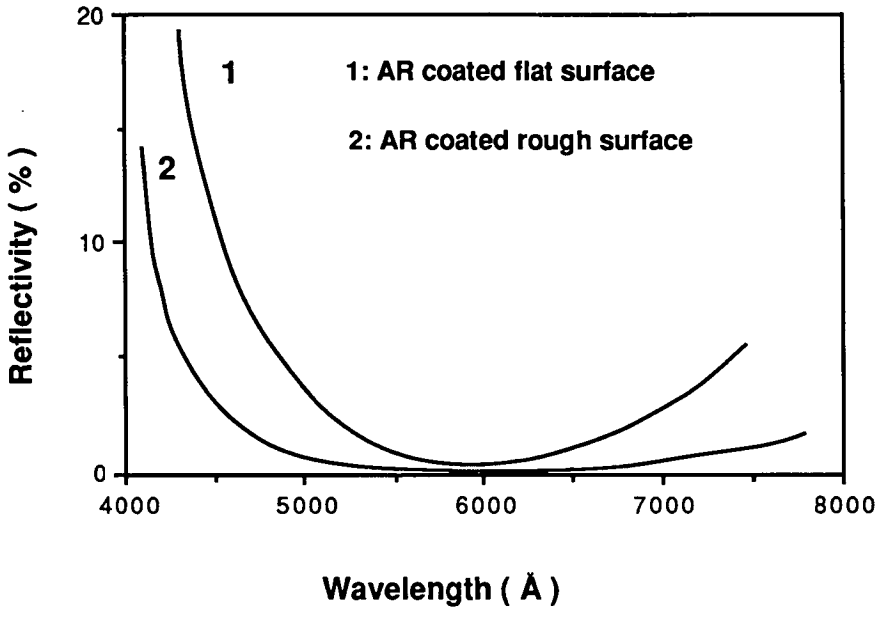


Fig. 6.2.1. Reflectivity with respect to wavelength for flat and roughened surfaces.

6.3 Reduction of surface recombination

Reducing the surface recombination at the junction interfaces will improve conversion efficiency. We have chosen the n/n+(100) Si wafer for this project because its bulk resistivity was low and ohmic contacts could be made easily to the wafer.. The thickness of n-type epi-layer used was 10 μm and the resistivity was 10-15 Ohm-cm. Typically, Al/Ti was coated on the n^+ backside and Al was alloyed on the frontside of the wafer. The n+ and the p+ used in the multiple junctions, shown in Fig. 6.3.1, would reduce surface recombination at the contact interfaces such that the electrons at the front surface would be kicked back into the bulk by p/p+ interface field, and that the holes at the back surface likewise would be kicked back into bulk by the n/n^+ interface field. Therefore, the generated electron-hole pairs would be

prevented from recombining at the interfaces and would contribute towards the photocurrent rather than being absorbed as a current leakage at the interfaces.

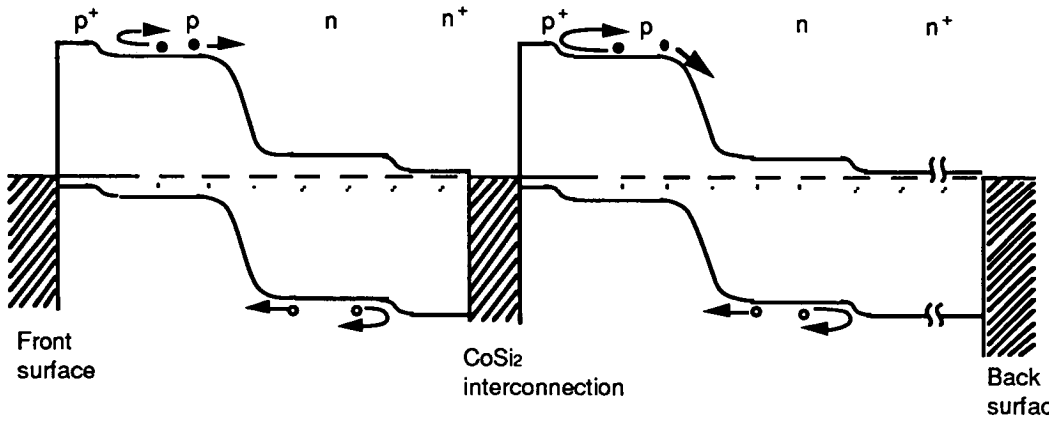


Fig. 6.3.1. Energy band diagram for reducing surface recombination in double p-n junctions with a $CoSi_2$ interconnect.

6.4 Multiple p-n junctions

We have so far fabricated three high-quality p-n junctions connected in series by $CoSi_2$ layers with resistivity as low as 10^{-5} Ohm-cm. However, we need to fabricate several more similar p-n junction layers (say, a total of ten p-n junctions) before the combined thickness is large enough for a practical determination of conversion efficiency with a laser beam. To accomplish at least ten junctions, the growth rate must be maintained at about 10 micron/hour and the quality of the respective epitaxial layers must not degrade significantly in growing two to ten junctions. Our research, as described in section 5, showed that the crystallinity (measured by RBS) of the subsequent epitaxial layers degrades by about 5% per layer. This means the conversion efficiency will degrade as the number of layers increases. We estimate that ten to twenty layers will be the limit before the degradation becomes unacceptable. However, a practical laser converter can still be fabricated by stacking several 10-junction (or 20-junction) mini-stacks together. Thus, one key to achieving multiple junctions in a reasonable growth time is to increase the rate of junction growth over the rate that we have developed so far, while maintaining the quality of epitaxy through out. This can be accomplished with our existing process by using more powerful e-beam sources for evaporating the Co and Si in conjunction with a larger growth chamber volume cooled by liquid nitrogen to prevent cross contamination during the high rate of growth. The rest of the growth procedure will be the same as that developed so far.

7.0 CONCLUSION

We have developed an MBE process for fabricating multiple p-n junctions connected in series by pinhole-free, low-resistivity $CoSi_2$ layers. The resultant structure of three p-n junctions connected by two single-crystal $CoSi_2$ layers showed excellent current-voltage characteristics has demonstrated the feasibility of fabricating high-conversion-efficiency laser converter.

For the MBE process, high-temperature e-beam sources for Si and Co have been especially developed. The in-situ doping developed using conventional effusion sources designed for low cross contamination during prolonged growth has achieved the required 10^{17} /cm^3 level of doping in the n-type and p-type layers. Boron was used for the p-type while Sb for the n-type dopant. The process, making use of the small (< 1.2%) lattice mismatch between $CoSi_2$ and Si, could achieve high-quality epilayers, providing a relatively straightforward procedure for fabricating all the multiple and connecting layers as a single MBE process with one pumpdown. During development, high-quality p-n junctions and low-resistivity $CoSi_2$ layers with resistivity as low as 10^{-5} Ohm-cm have been demonstrated separately and in a series combination.

We have achieved well-defined p-n junctions connected by $CoSi_2$ layers by maintaining a low growth temperature ($\leq$ 700 °C) and a low growth rate (< 0.5 μm/hr), keeping the interdiffusion to a negligible level throughout growth. The low growth temperature and rate also produced negligible pinholes in the $CoSi_2$ layers. Under these conditions, the typical growth run took over eight hours to fabricate a stack of two to four p-n junctions. For the first time a stack of three p-n junctions connected by two 10^{-5} Ω-cm $CoSi_2$ layers has been achieved meeting the high conversion efficiency requirement.

For a practical determination of conversion efficiency with a laser beam we need to fabricate at least 10 p-n junction layers, for which the growth rate must be maintained at about 10 micron/hour and the quality of the respective epitaxial layers must not degrade significantly in growing two to ten junctions. Based on our process, this can be achieved by using more powerful e-beam sources for evaporating the Co and Si in conjunction with a larger growth chamber volume cooled by liquid nitrogen to prevent cross contamination during the high rate of growth. The rest of the growth procedure will be the same as that developed so far. A practical laser converter can then be fabricated by stacking several 10-junction (or 20-junction) mini-stacks together.

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Hamilton Lu
Scott Wang
W. S. Chan

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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3152 Kashiwa Street
Torrance, CA 90505-4011

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13. ABSTRACT *(Maximum 200 words)*

A laser-energy converter, fabricated by molecular beam epitaxy (MBE), has been developed. This converter is a stack of vertical p-n junctions connected in series by low-resistivity, lattice matched $CoSi_2$ layers to achieve a high conversion efficiency. Special high-temperature electron-beam (e-beam) sources have been developed especially for the MBE growth of the junctions and $CoSi_2$ layers. Making use of the small (< 1.2 percent) lattice mismatch between $CoSi_2$ and Si layers, high-quality and pinhole-free epilayers have been achieved, providing a capability of fabricating all the junctions and connecting layers as a single growth process with one pumpdown. Well-defined multiple p-n junctions connected by $CoSi_2$ layers were accomplished by employing a low growth temperature (< 700° C) and a low growth rate (< 0.5 μm/hr). Producing negligible interdiffusion, the low growth temperature and rate also produced negligible pinholes in the $CoSi_2$ layers. For the first time, a stack of three p-n junctions connected by two 10^{-5} Ω-cm $CoSi_2$ layers has been achieved, meeting the high conversion efficiency requirement. This process can now be optimized for high growth rate to form a practical converter with 10 p-n junctions in the stack.

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